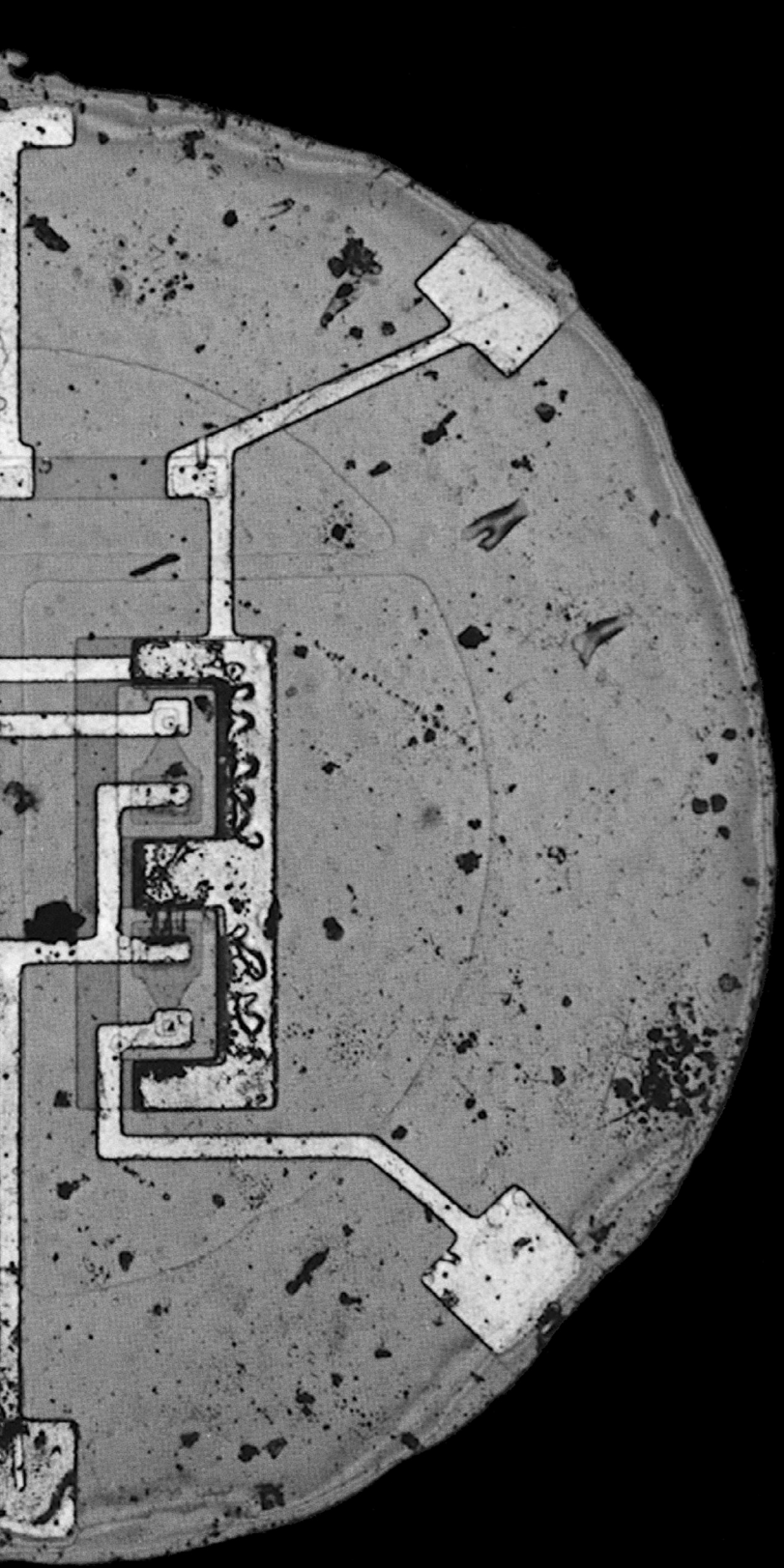

IC at fifty

COMPUTER HISTORY MUSEUM

Milestones in the development of transistors and integrated circuits selected from The Silicon Engine *online exhibit*

IC at fifty

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www.computerhistory.org

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Cover image: Fairchild Semiconductor Micrologic type “F” flip-flop, circa 1960.
Credit: Fairchild Camera & Instrument Corporation.

Revision #85. Set in Chaparral.

Foreword

IC at fifty is a publication of the Computer History Museum's *Salute to the Semiconductor* program featuring a year of events and commemorative activities related to the history and growth of the integrated circuit (IC) and its impact on society. Major funding for this program is generously provided by the Gordon and Betty Moore Foundation and Intel Corporation. Additional funding for specific events is provided by the National Semiconductor Foundation, a charitable fund at the Silicon Valley Community Foundation.

Beginning May 2, the Computer History Museum is partnering with the Chemical Heritage Foundation, the IEEE Santa Clara Valley Section and the National Inventors Hall of Fame to host a week of celebratory activities honoring the 50th anniversary of the activities that led to the modern integrated circuit. The late 1950s and early 1960s was an extraordinary period of development in semiconductor electronics. Military interest in, and the semiconductor industry's pursuit of diverse approaches to miniaturizing transistor-based systems took off in the second half of the 1950s. 1959 saw a burst of intellectual activity across the industry aimed at improved approaches to microcircuitry. Jack Kilby of Texas Instruments, along with Jean Hoerni and Robert Noyce of Fairchild Semiconductor, and others, filed patent applications that held keys to the development of the monolithic integrated circuit. Jay Last's team at Fairchild, which would create the first planar integrated circuits, also began their efforts in 1959.

As the basic building block of digital electronics, the integrated circuit has profoundly transformed societies across the globe. Reflecting this impact, Isaac Asimov once described the innovation of the integrated circuit as "the most important moment since man emerged as a life form." *IC at fifty* is based on the text of selected milestones from the Computer History Museum's *The Silicon Engine* online semiconductor exhibit that focuses on the invention of the transistor and the technologies and events that enabled the transition to integrated circuits and their central role in the development of computers.

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IC at fifty design
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About The Silicon Engine

Developed by members of the Computer History Museum's Semiconductor Special Interest Group in cooperation with the curatorial and technology staff, *The Silicon Engine* was the first comprehensive online presentation of the history of semiconductor technology as applied to computing applications to be developed by a major institution. In addition to the milestones selected for this booklet, the website includes numerous primary and secondary references, many additional photographs, biographies of the people and their companies and institutions, a glossary of semiconductor terms, and extensive student and teacher resource materials. *The Silicon Engine* was made possible by grants from the Gordon and Betty Moore Foundation and the House Family Foundation.

Microelectronic semiconductor silicon computer "chips" have grown in capability from a single transistor in the 1950s to over one billion transistors per chip on today's advanced microprocessor and memory integrated circuits (ICs). From the first documented semiconductor effect in 1833 to the transition from discrete transistors to ICs through the late 1970s, *The Silicon Engine* is an online exhibit that chronicles important milestones in the evolution of these extraordinary engines that power the computing and communications revolution of the information age.

The Silicon Engine is posted on the Computer History Museum website at *www.computerhistory.org/semiconductor*.

About the Computer History Museum

The Computer History Museum (CHM) is dedicated to the preservation and celebration of the computing revolution and its worldwide impact on the human experience. It is home to the largest international collection of computing artifacts in the world, encompassing computer hardware, software, documentation, ephemera, photographs and moving images.

CHM brings computer history to life through an acclaimed speaker series, dynamic website, onsite tours, as well as physical and online exhibits. We have a wide variety of programs and participation opportunities. Support computer history by becoming involved as a member, attendee, donor, corporate sponsor or volunteer.

Current exhibits in the Museum:

- **Charles Babbage's Difference Engine №2**
  Designed in the 1840s, the Engine is a stunning display of Victorian mechanics and an arresting spectacle of automatic computing. It consists of 8,000 bronze, cast iron and steel parts, weighs 5 tons, and measures 11 ft. long and 7 ft. high.
- **Visible Storage**
  The Visible Storage gallery features over 600 unique artifacts – from rare slide rules and mechanical calculators to the earliest one-of-kind computers, vintage PCs and exotic supercomputers.
- **Mastering the Game: A History of Computer Chess**
  Our History of Chess exhibit examines computing's five-decade-long quest to build a computer to challenge the best chess players.
- **Innovation in the Valley**
  Learn about the innovators of computing technology in Silicon Valley who have changed our world, including local giants Apple, Cisco, HP, Intel and Sun.
- **Computer History: The First 2,000 Years**
  Our upcoming signature exhibit.

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Lecture videos: *youtube.com/computerhistory*
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Open hours:

Wed	12 pm–4 pm
Thu	12 pm–4 pm
Fri	12 pm–4 pm
Sat	11 am–5 pm
Sun	12 pm–4 pm

Timeline

1947	Invention of the point-contact transistor
1948	Conception of the junction transistor
1951	First grown-junction transistors fabricated Development of zone refining
1953	Transistorized computers emerge
1954	Silicon transistors offer superior operating characteristics Diffusion process developed for transistors
1955	Development of oxide masking Photolithography techniques are used to make silicon devices
1956	Silicon comes to Silicon Valley
1958	Silicon mesa transistors enter commercial production All-semiconductor "Solid Circuit" is demonstrated
1959	Invention of the "planar" manufacturing process Practical monolithic integrated circuit concept patented
1960	First planar integrated circuit is fabricated Metal Oxide Semiconductor (MOS) transistor demonstrated Epitaxial deposition process enhances transistor performance
1961	Silicon transistor exceeds germanium speed
1962	Aerospace systems are the first applications for ICs in computers

1963	Complementary MOS circuit configuration is invented Standard logic IC families introduced
1964	Hybrid microcircuits reach peak production volumes First commercial MOS ICs introduced The first widely-used analog integrated circuit is introduced
1965	"Moore's Law" predicts the future of integrated circuits Large computers demand specialty integrated circuits Read-Only Memory is the first dedicated IC memory configuration
1966	Semiconductor RAMs developed for high-speed storage Computer-Aided Design tools developed for ICs
1967	Application-specific integrated circuits employ Computer-Aided Design
1968	Dedicated current source IC integrates a data conversion function Silicon gate technology developed for ICs
1969	Schottky-barrier diode doubles the speed of TTL memory & logic
1970	MOS dynamic RAM competes with magnetic core memory on price
1971	Reusable programmable ROM introduces iterative design flexibility Microprocessor condenses CPU function onto a single chip
1974	General-purpose microcontroller family is announced Scaling of IC process design rules is quantified

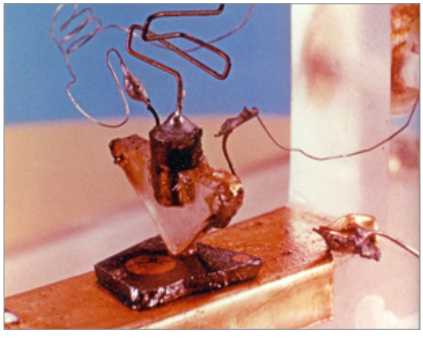
1947

PAGE 8

Invention of the point-contact transistor

Nielsen

↑ Bardeen, Brattain, and Shockley (seated) on the cover of Electronics magazine September 1948 "Crystal Triode" issue



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↑ Bardeen and Brattain's first point-contact transistor

John Bardeen & Walter Brattain achieve transistor action in a germanium point-contact device in December 1947.

Encouraged by Executive Vice President Mervin Kelly, William Shockley returned from wartime assignments in early 1945 to begin organizing a solid-state physics group at Bell Labs. Among other things, this group pursued research on semiconductor replacements for unreliable vacuum tubes and electromechanical switches then used in the Bell Telephone System. That April Shockley conceived a "field-effect" amplifier and switch based on the germanium and silicon technology developed during the war, but it failed to work as intended. A year later, theoretical physicist John Bardeen suggested that electrons on the semiconductor surface might be blocking penetration of electric fields into the material, negating any effects. With experimental physicist Walter Brattain, Bardeen began researching the behavior of these "surface states."

On December 16, 1947, their research culminated in the first successful semiconductor amplifier. Bardeen and Brattain applied two closely-spaced gold contacts held in place by a plastic wedge to the surface of a small slab of high-purity germanium. The voltage on one contact modulated the current flowing through the other, amplifying the input signal up to 100 times. On December 23, they demonstrated their device to lab officials—in what Shockley deemed "a magnificent Christmas present."

Named the "transistor" by electrical engineer John Pierce, Bell Labs publicly announced the revolutionary solid-state device at a press conference in New York on June 30, 1948. A spokesman claimed that "it may have far-reaching significance in electronics and electrical communication." Despite its delicate mechanical construction, many thousands of units were produced in a metal cartridge package as the Bell Labs "Type A" transistor.

Conception of the junction transistor

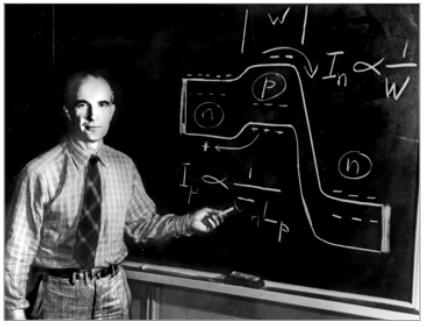
1948

William Shockley conceives an improved transistor structure based on a theoretical understanding of the *p-n* junction effect.

After Bardeen and Brattain's December 1947 invention of the point-contact transistor (PAGE 8), Bell Labs physicist William Shockley began a month of intense theoretical activity. On January 23, 1948 he conceived a distinctly different transistor based on the *p-n* junction discovered by Russell Ohl in 1940. Partly spurred by professional jealousy, as he resented not being involved with the point-contact discovery, Shockley also recognized that its delicate mechanical configuration would be difficult to manufacture in high volume with sufficient reliability.

Shockley also disagreed with Bardeen's explanation of how their transistor worked. He claimed that positively charged holes could also penetrate through the bulk germanium material—not only trickle along a surface layer. Called "minority carrier injection," this phenomenon was crucial to operation of his junction transistor, a three-layer sandwich of *n*-type and *p*-type semiconductors separated by *p-n* junctions. This is how all "bipolar" junction transistors work today.

On February 16, 1948, physicist John Shive achieved transistor action in a sliver of germanium with point contacts on opposite sides, not next to each other, demonstrating that holes were indeed flowing through the germanium. Shockley applied for a patent on the junction transistor that June and published his detailed theory of its operation in 1949. Still, it was two more years before Bell Labs scientists and engineers developed processes that allowed his junction transistor to be manufactured in production quantities (PAGE 10).



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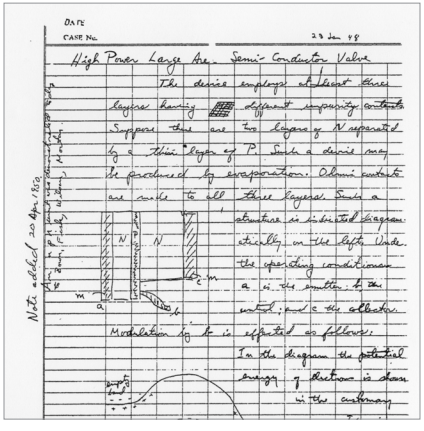
↑ William Shockley describing junction transistor theory



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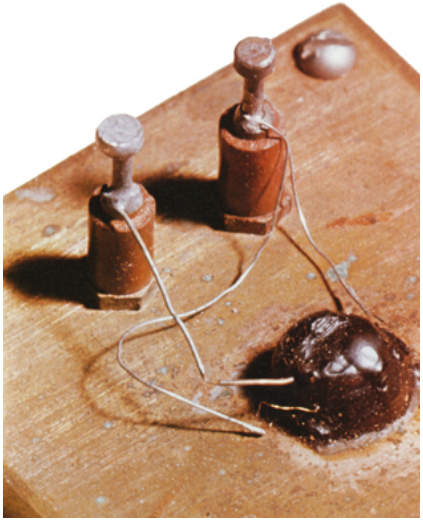
↑ A page from Shockley's lab notebook describing his junction idea

1951

PAGE 10

First grown-junction transistors fabricated



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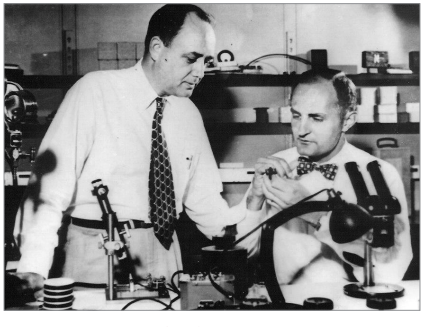
↑ The first junction transistor made by Sparks in 1949



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↑ Gordon K. Teal (left) and Morgan Sparks at Bell Laboratories, 1951

Gordon Teal grows large single crystals of germanium and works with Morgan Sparks to fabricate an *n-p-n* junction transistor.

After William Shockley's theories about *p-n* junctions had been validated by tests (PAGE 9), fabricating a working junction transistor still presented formidable challenges. The main problem was lack of sufficiently pure, uniform semiconductor materials. Bell Labs chemist Gordon Teal argued that large, single crystals of germanium and silicon would be required, but few—including Shockley—were listening.

With little support from management, Teal built the needed crystal-growing equipment himself, with help from mechanical engineer John Little and technician Ernest Buehler. Based on techniques developed in 1917 by the Polish chemist Jan Czochralski, he suspended a small "seed" crystal of germanium in a crucible of molten germanium and slowly withdrew it, forming a long, narrow, single crystal. Shockley later called this achievement "the most important scientific development in the semiconductor field in the early days."

Employing this technique, Bell Labs chemist Morgan Sparks fabricated *p-n* junctions by dropping tiny pellets of impurities into the molten germanium during the crystal-growing process. In April 1950, he and Teal began adding two successive pellets into the melt, the first with a *p*-type impurity and the second *n*-type, forming *n-p-n* structures with a thin inner, or base, layer. A year later, such "grown-junction transistors" surpassed the best point-contact transistors in performance. Bell Labs announced this advance on July 4, 1951 in a press conference featuring Shockley.

Development of zone refining

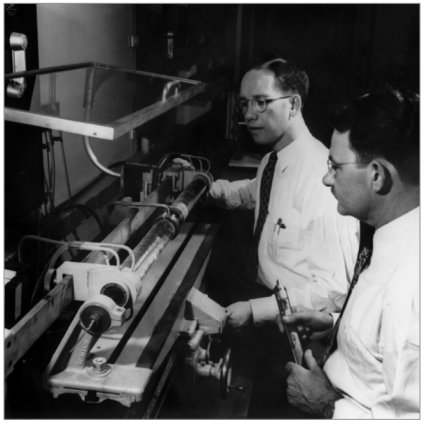
1951

William Pfann and Henry Theurer develop zone refining techniques for production of ultra-pure semiconductor materials.

A crucial semiconductor technology developed at Bell Labs in the early 1950s is zone refining, which leads to ultra-pure samples of germanium and silicon with impurities as low as one part in ten billion—equivalent to a pinch of salt in three freight cars of sugar. Such ultra-pure semiconductor samples allow exquisite control of *n*-type and *p*-type regions by adding small amounts of impurities.

Chemical engineer William Pfann pioneered zone refining in 1950–51. By repeatedly passing a long tube filled with germanium horizontally through a series of electrical heating coils, he melted portions of the germanium and allowed them to recrystallize. The newly crystalline material was purer than what came before, while impurities became steadily concentrated in the molten portions, which were swept away to the tube's ends.

This technique did not work for silicon, however, because it melts at higher temperatures (1415°C versus 937°C for germanium) and reacts with almost all other materials. Beginning in 1952, Bell Labs chemist Henry Theurer developed a variation on this technique called float-zone refining in which a rod of silicon clamped at both ends passes vertically through a heating coil. The small molten segment remains fixed in place between the solid portions of the rod due to surface tension. Using steam refining to remove the most stubborn impurities, such as boron, he produced silicon with impurity levels below one part per billion in early 1955. The process was developed independently at two other laboratories; by P. H. Keck and M. J. E. Golay, at the U. S. Army Signal Corps, Fort Monmouth, NJ and by R. Emeis working under the direction of Eberhard Spenke at Siemens in Pretzfeld, West Germany.



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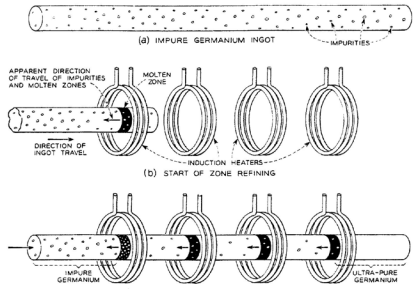
↑ William Pfann and Jack Scaff with early zone-refining equipment



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↑ Illustration of the process of zone refining

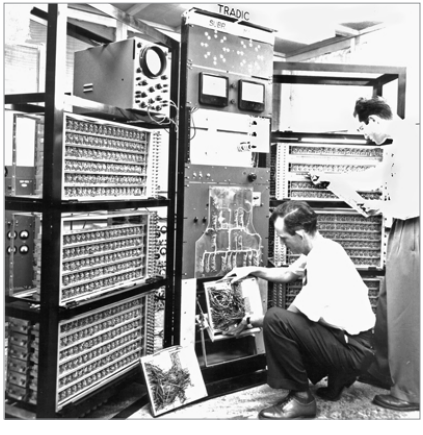
1953

Transistorized computers emerge

PAGE 12

U. S. National Bureau of Standards

↑ The SEAC computer operator's station



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↑ J. H. Felker and J. R. Harris work on the Bell Labs TRADIC computer

A transistorized computer prototype demonstrates the small size and low-power advantages of semiconductors compared to vacuum tubes.

During the 1950s, semiconductor devices gradually replaced vacuum tubes in digital computers. By 1960, new designs were fully transistorized. Operational in April 1950, the National Bureau of Standards Eastern Automatic Computer (SEAC) employed 10,500 germanium diodes and 747 vacuum tubes.

Working under Tom Kilburn at Manchester University, Richard Grimsdale and Douglas Webb, demonstrated a prototype transistorized computer on November 16, 1953. The 48-bit machine used 92 point-contact transistors and 550 diodes fabricated by STC, the U. K. arm of ITT. An enhanced version with 250 junction transistors was completed in 1955. The Metropolitan Vickers Electrical Company manufactured six units as the Metrovick 950, which they used commercially within the company from 1956.

Jean H. Felker led a Bell Labs team including engineer James R. Harris that designed and built a fully transistorized computer dubbed TRADIC (TRAnsistor DIgital Computer) for the U. S. Air Force in 1954. Involving about 700 point-contact transistors and over 10,000 diodes, the prototype operated at 1 MHz while requiring less than 100 watts of power. A lighter airborne version (Flyable TRADIC) using junction transistors replaced an analog computer for navigation and bombing control in a C-131 aircraft. Led by William Papian, in April 1956 members of the Advanced Development Group of MIT Lincoln Labs used fast germanium switching transistors from Philco Corporation to build a 5 MHz general-purpose digital computer known as TX-0 (Transistor Experimental). Also in 1956, Japan's first transistorized computer, the ETL Mark III, using 130 point-contact transistors and 1800 diodes was built under the direction of Hiroshi Wada at the Electrotechnical Laboratory in Tokyo.

Silicon transistors offer superior operating characteristics

Morris Tanenbaum fabricates the first silicon transistor at Bell Labs but Texas Instruments' engineers build and market the first commercial devices.

For the first six years of their existence, transistors had all been made with germanium. Although this element is much easier to work with than silicon and allows higher-frequency operation, solid-state devices made with it have far worse leakage currents in the "off" condition—an anathema for computer logic. They are also restricted to 0 to 70°C operation, which limits their use in rugged applications. Silicon devices that function from –55 to 125°C became possible after Dupont began supplying high-purity "semiconductor-grade" material. In January 1954 Bell Labs chemist Morris Tanenbaum fashioned the first silicon transistor using a variation on Morgan Sparks and Gordon Teal's grown-junction technique.

But the Labs did not pursue the process further, thinking it unattractive for commercial production, which allowed Texas Instruments (TI) to claim credit for this breakthrough several months later. Having left Bell Labs to organize a research lab at TI, Teal hired a team of scientists and engineers led by chemist Willis Adcock to work on silicon transistors. Employing high-purity Dupont silicon, they made their first successful silicon transistor—an *n-p-n* structure using the grown-junction technique—on April 14, 1954. Unaware of Tanenbaum's work, Teal presented this achievement on May 10 at an Institute of Radio Engineers conference in Dayton, Ohio, creating a sensation by announcing that silicon transistors were in production and available for sale. With little competition, TI dominated the silicon-transistor market for the next few years and made significant inroads into Raytheon's position as the largest merchant market supplier of transistors. By the end of the 1950s, silicon had become the industry's preferred semiconductor material.

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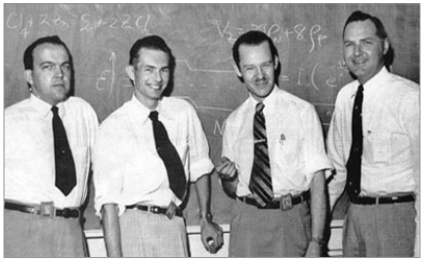
↑ Morris Tanenbaum (left) and Charles Lee (right) at Bell Labs



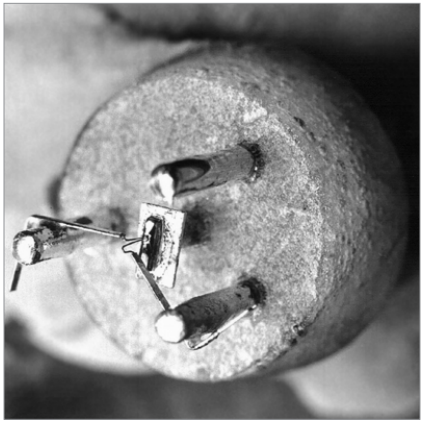
Texas Instruments, Inc.

↑ TI's 1954 silicon-transistor team: W. Adcock, M. Jones, E. Jackson, and J. Thornhill

1954

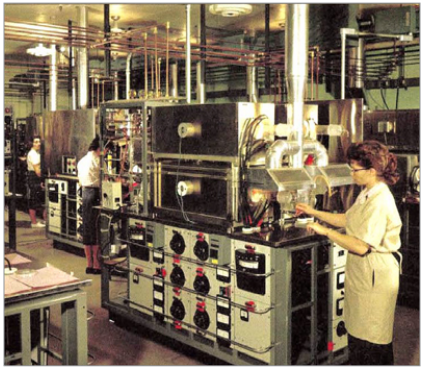
PAGE 14

Diffusion process developed for transistors



Morris Tanenbaum

↑ One of the first diffused-base silicon transistors at Bell Labs



Fairchild Camera & Instrument Corporation

↑ Silicon transistor wafer diffusion furnaces at Fairchild in 1960

Following the production of solar cells using high-temperature diffusion methods, Charles Lee and Morris Tanenbaum apply the technique to fabricate high-speed transistors.

Beginning in 1952, Bell Labs chemist Calvin Fuller demonstrated how impurities could be introduced into germanium and then silicon by exposing them to high-temperature gases containing desired dopants. By adjusting the time and temperature of exposure, he could precisely control the amount of impurities introduced and their penetration depth to accuracies of better than one micrometer—far better than achievable with grown-junction techniques.

Working with engineer Daryl Chapin and physicist Gerald Pearson in early 1954, Fuller diffused a layer of boron atoms into wafers of *n*-type silicon, forming large-area *p-n* junctions just beneath the surface. By shining light on these junctions, they generated a strong electric current via the photovoltaic effect discovered by Ohl in 1940, getting energy conversion efficiencies up to 6 percent. Bell Labs announced this solar cell, dubbed the "Solar Battery," on 26 April 1954. By the late 1950s, solar cells were powering rural telephone systems and space satellites.

Later that year Charles Lee used diffusion to make transistors with base layers only a micrometer thick; they could operate at frequencies up to 170 MHz—ten times higher than earlier devices. And in March 1955, employing silicon wafers into which Fuller had diffused two different impurities to form a three-layer *n-p-n* sandwich, chemist Morris Tanenbaum and his technician D. E. Thomas fabricated silicon diffused-base transistors. In January 1956, Bell Labs held a third symposium on transistor technology specifically devoted to these and other diffusion techniques.

Development of oxide masking

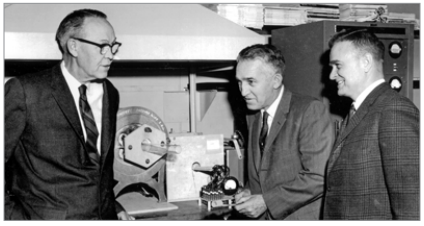
1955

Carl Frosch and Lincoln Derick grow a silicon dioxide film on wafers to protect their surface and allow controlled diffusion into the underlying silicon.

In early 1955, Bell Labs researchers encountered a major problem with pitting on the surface of silicon wafers during high-temperature diffusion. This problem was overcome by chemist Carl Frosch during a serendipitous accident in which the hydrogen gas carrying impurities through the diffusion furnace briefly caught fire, introducing water vapor into the chamber. The resulting "wet-ambient" diffusion method had covered the silicon surface with a layer of glassy silicon-dioxide (SiO_2).

Developed further by Frosch and his technician Lincoln Derick in the ensuing months, this technique allowed semiconductor workers to seal and protect silicon wafers during the diffusion process. The two men established what impurities, such as gallium, could penetrate the oxide layer and which others (boron and phosphorus, for example) could not. They also demonstrated how to etch small openings in the layer in order to diffuse these impurities into selected portions of the silicon surface and pattern it precisely with tiny *n*-type and *p*-type regions. In 1957, they patented and published this extremely important technique.

The silicon-dioxide layer soon became essential to manufacturing transistors and later integrated circuits in high volume production via the planar processing method, (PAGE 20) which employs this layer to protect sensitive *p-n* junctions in the silicon from contamination. It also doubles as an effective insulating layer atop which metal interconnections are deposited. More than any other single factor, silicon's supple, adaptable oxide layer has established it as by far the dominant material used in microchip manufacturing.



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↑ Calvin Fuller, Carl Frosch and Lincoln Derick with an early diffusion furnace

CHM collection: Photo gift of Forrest Trumbore

↑ Slide of "The End" etched on a silicon wafer was used by Frosch to conclude his presentations

1955

PAGE 16

Photolithography techniques are used to make silicon devices

Semiconductor Equipment and Materials International (SEMI)

↑ Burt Wheeler developed the Mann photorepeater for making masks

Intel Corporation

↑ Hand cutting an IC design onto rubylith material for creating the pattern to be optically shrunk onto a photographic mask – early 1970s

Jules Andrus and Walter Bond adapt photoengraving techniques from printing technology to enable precise etching of diffusion "windows" in silicon wafers.

In 1955, Jules Andrus and Walter L. Bond at Bell Labs began adapting existing photolithographic (also called photoengraving) techniques developed for making patterns on printed circuit boards to produce much finer, more intricate designs on silicon in wafers using Frosch and Derick's silicon-dioxide layer (PAGE 15). After applying a photosensitive coating or "resist" on the layer and exposing the desired pattern on this coating through an optical mask, precise window areas were defined in the layer and opened by chemical etching where unexposed resist had been washed away. Impurities were diffused through these openings into the underlying silicon to establish the zones of *n*-type and *p*-type silicon needed in semiconductor devices.

In an early attempt to miniaturize electronic circuits in 1957, Jay Lathrop and James Nall of the U. S. Army's Diamond Ordnance Fuse Laboratories in Maryland patented photolithographic techniques used to deposit thin-film metal strips about 200 micrometers wide to connect discrete transistors on a ceramic substrate. They also used these techniques to etch holes in silicon dioxide to fabricate diode arrays. In 1959, Lathrop joined Texas Instruments, working for Jack Kilby, and Nall went to Fairchild Semiconductor.

Following up on this pioneering work, Jay Last and Robert Noyce built one of the first "step-and-repeat" cameras at Fairchild in 1958 to make many silicon identical transistors on a single wafer using photolithography. In 1961, the David W. Mann division of GCA Corporation was the first firm to make commercial step and repeat mask reduction devices (photo-repeaters). Photolithography remains an essential step in semiconductor manufacturing today, with feature sizes below 0.1 micrometer becoming commonplace.

Silicon comes to Silicon Valley

1956

Shockley Semiconductor Laboratory develops Northern California's first prototype silicon devices while training young engineers and scientists for the future Silicon Valley.

In September 1955, William Shockley and Arnold Beckman agreed to found the Shockley Semiconductor Laboratory as a Division of Beckman Instruments "to engage promptly and vigorously in activities related to semiconductors." Shockley rented a building at 391 South San Antonio Road in Mountain View, California, and began recruiting "the most creative team in the world for developing and producing transistors." He attracted extremely capable engineers and scientists, including Gordon Moore and Robert Noyce, who learned about and developed technologies and processes related to silicon and diffusion while working there. In December 1956, Shockley shared the Nobel Prize in Physics for inventing the transistor, but his staff was becoming disenchanted with his difficult management style. They also felt the company should pursue more immediate opportunities for producing silicon transistors rather than the distant promise of a challenging four-layer *p-n-p-n* diode he had conceived at Bell Labs for telephone switching applications.

After unsuccessfully asking Beckman to hire a new manager, eight Shockley employees—including Moore and Noyce plus Julius Blank, Victor Grinich, Jean Hoerni, Eugene Kleiner, Jay Last and Sheldon Roberts—resigned in September 1957 and founded the Fairchild Semiconductor Corporation in Palo Alto. Many other employees, from technicians to PhDs, soon followed. Over the next decade, Fairchild grew into of the most important and innovative companies in the semiconductor industry, laying the technological and cultural foundations of Silicon Valley while spinning off dozens of high-tech start-ups, including Advanced Micro Devices (AMD) and Intel. Shockley continued pursuing his four-layer diode but his company never realized a profit. Beckman sold the operation to Clevite Corporation in 1960. Shockley became a professor of electrical engineering and applied science at Stanford University.

Intel Corporation

↑ Toasting Shockley's Nobel Prize award at Rickey's Hotel, Palo Alto, CA. Celebrants include G. Moore, S. Roberts, R. Noyce, and J. Last

Hans Quéisser

↑ The Shockley Semiconductor Laboratory facility, Mountain View, California, circa 1960

1958

PAGE 18

Silicon mesa transistors enter commercial production

Wayne Miller, Magnum Photos

↑ "The Fairchild Eight" founders pose in the company lobby, circa 1960

Fairchild Camera and Instrument Corporation

↑ Fairchild Semiconductor wafer diffusion area, Palo Alto, circa 1958

Fairchild Semiconductor produces double-diffused silicon mesa transistors to meet demanding aerospace applications.

In early 1958, Fairchild Semiconductor procured its first order, for 100 transistors at $150 apiece from IBM's Federal Systems Division. No established manufacturer could meet its exacting specifications for a high-voltage silicon transistor to drive magnetic core memory in the B-70 on-board computer. Two development projects were pursued in parallel. A team led by Gordon Moore developed an *n-p-n* transistor and by Jean Hoerni, which worked on a *p-n-p* device.

In just five months, the founders (PAGE 17) set up a crystal-growing operation (Sheldon Roberts), developed photolithographic masking techniques using 16 mm movie-camera lenses (Jay Last, Robert Noyce), established the aluminum characteristics needed for making electrical contacts (Moore), and built their own manufacturing and test equipment (Julius Blank, Victor Grinich, Eugene Kleiner) at their Palo Alto facility. Building on their exposure to Bell Labs techniques (PAGE 14) at Shockley, they developed the first commercial double-diffused (emitter and base) silicon mesa transistor, so named for its raised plateau-like structure. After successful delivery of the Moore team's *n-p-n* transistor, the device was introduced as type 2N697 to great acclaim at the Wescon trade show in August 1958.

Autonetics selected the device for a guidance-and-control system on the Minuteman ballistic missile, the largest defense program of the era. In late 1958, a potential reliability problem put the new firm's survival at stake. Tiny particles flaking off the inside of the metal package threatened to short across exposed junctions on the mesa structure. Hoerni's solution, the famous planar process (PAGE 20), revolutionized the industry by covering the exposed junction with silicon dioxide.

All-semiconductor "Solid Circuit" is demonstrated

1958

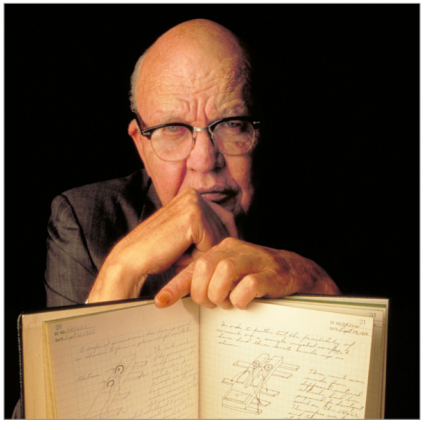
PAGE 19

Jack Kilby produces a microcircuit with both active and passive components fabricated from semiconductor material.

As computer systems grew more complex, engineers sought simpler ways to interconnect the thousands of transistors they employed. Government agencies funded micro-module and multi-chip hybrid circuit projects in search of a solution to this "tyranny of numbers" problem. At England's Royal Radar Establishment in 1952, G. W. A. Dummer proposed: "With the advent of the transistor (and the work in semiconductors in general), it seems now possible to envisage electronic equipment in a solid block."

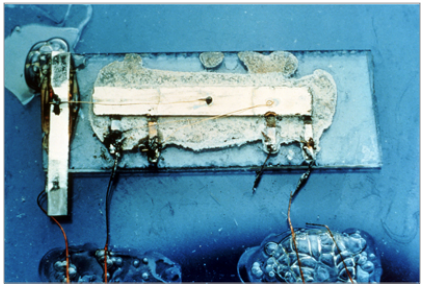
Several projects resulted in devices that replaced multiple discrete components. At RCA, Harwick Johnson patented a single-chip oscillator and Torkel Wallmark and Sanford Marcus designed shift registers and unipolar logic gates. Arthur D'Asaro and Ian Ross of Bell Labs built a four-stage counter for telephone applications. Joe Logue and Rick Dill of IBM built a double base diode structure counter. Yasuro Tarui of Japan's MITI filed a patent describing bipolar and FET transistors on one chip. While achieving various degrees of functionality, none of these ideas yielded a solution to the challenge of general-purpose system integration.

On September 12, 1958, Jack Kilby of Texas Instruments built a circuit using germanium mesa *p-n-p* transistor slices he had etched to form transistor, capacitor, and resistor elements. Using fine gold "flying-wires" he connected the functions to form an oscillator circuit. One week later he demonstrated an amplifier. TI announced Kilby's "solid circuit" concept in March 1959 and introduced its first commercial device in March 1960, the Type 502 Binary Flip-Flop priced at $450 each. However the flying-wire interconnections were not a practical production technique nor did they address the tyranny of numbers issue. In October 1961, they were replaced by the Series 51 DCTL "fully-integrated circuit" family using planar technology (**PAGE 21**).



Texas Instruments, Inc.

↑ Jack Kilby with his lab notebook open at his first solid circuit drawing



Texas Instruments, Inc.

↑ Kilby's original germanium multi-chip "solid-circuit" oscillator

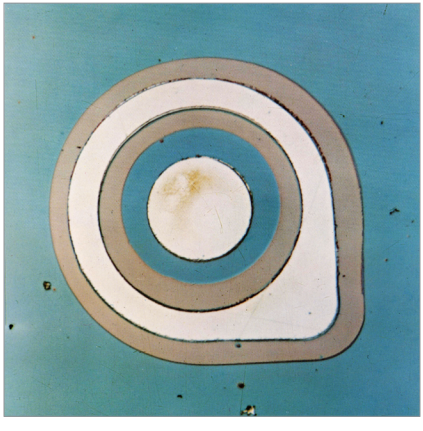
1959

PAGE 20

Invention of the "planar" manufacturing process

Semiconductor Equipment and Materials International

↑ Jean Hoerni with transistor geometry in the background



Fairchild Camera and Instrument Corporation

↑ Photomicrograph of a Model 2N1613 planar transistor

Jean Hoerni develops the planar process to solve reliability problems of the mesa transistor, thereby revolutionizing semiconductor manufacturing.

Seeking a solution to reliability issues with the mesa transistor (PAGE 18), Fairchild physicist Jean Hoerni recalled an idea he had recorded in December 1957 - a new process in which the oxide layer is left in place on the silicon wafer to protect the sensitive *p-n* junctions underneath. Focused on getting its first devices into production, the company did not pursue the approach at that time. Due to concerns about possible contaminants, conventional wisdom required removing this layer after completion of oxide masking, thus exposing the junctions. Hoerni viewed the oxide instead as a possible solution—his "planar" approach, named after the flat topography of the finished device, would protect these junctions. After writing a patent disclosure in January 1959, he demonstrated a working planar transistor that March. The oxide layer was indeed found to protect the junctions, as Hoerni had predicted.

Planar devices also proved to have better electrical characteristics—particularly far lower leakage currents, which is critical in computer logic design. And they permitted fabrication of all the components of an integrated circuit from one side of a wafer (PAGE 22). Fairchild introduced the 2N1613 planar transistor commercially in April 1960 and licensed rights to the process across the industry. The billion-transistor integrated circuits of today rely on Hoerni's breakthrough idea. One historian has called it "the most important innovation in the history of the semiconductor industry."

While planar technology enabled silicon transistors to meet the stringent demands of the aerospace industry, semiconductor vendors continued to encounter new failure mechanisms with every major technology advance. Significant issues in the 1960s included "purple plague" on gold bonding wires, electromigration of aluminum interconnect lines, and MOS transistor stability (PAGE 30).

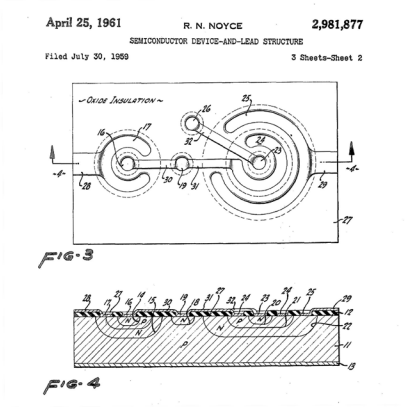
Practical monolithic integrated circuit concept patented

Robert Noyce builds on Jean Hoerni's planar process to patent a monolithic integrated circuit structure that can be manufactured in high volume.

Challenged by patent attorney John Ralls to identify other uses for Hoerni's planar process (PAGE 20), Fairchild co-founder Robert Noyce conceived the idea for a monolithic integrated circuit. By interconnecting diodes, transistors, resistors and capacitors diffused into the silicon with aluminum metal lines deposited on top of the protective oxide coating, one could configure complete electrical circuits on a single silicon chip. By eliminating the "flying-wire" connections, this would yield a practical method of manufacturing Jack Kilby's solid circuits (PAGE 19).

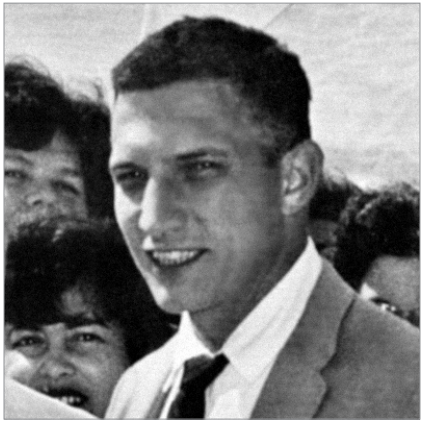
Noyce filed his "Semiconductor device-and-lead structure" patent in July 1959 and a team of Fairchild engineers produced the first working monolithic ICs in May 1960 (PAGE 22). They explored various schemes to electrically isolate devices from each other within the silicon wafer. Eventually they selected a reverse-biased *p-n* junction method patented by Kurt Lehovec of Sprague Electric. The planar method remains the fundamental approach used to produce ICs today.

Fairchild and TI engaged in litigation over IC patents for many years. The courts eventually ruled in Noyce's favor but by then the companies had already settled on a cross-license agreement that included a net payment to Fairchild. Kilby and Noyce both received the National Medal of Science and today are celebrated as co-inventors of the integrated circuit. Kilby is credited with building the first working circuit with all components formed using semiconductor material; Noyce with the metal-over-oxide interconnection scheme that yields a monolithic structure. As Noyce died in 1990, he did not share the Nobel Prize with Kilby a decade later, but many believe he would have had he lived.


April 25, 1961 R. N. NOYCE 2,981,877
SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE
Filed July 30, 1959 3 Sheets-Sheet 2
FIG. 3
FIG. 4

U.S. Patent Office

↑ Figure from Robert Noyce's basic IC patent



Fairchild Camera and Instrument Corporation

↑ Robert Noyce as General Manager of Fairchild in 1962

1960

First planar integrated circuit is fabricated

PAGE 22

Fairchild Camera & Instrument Corporation

↑ Jay Last with Gordon Moore in background

Fritz Goro, Time & Life Pictures

↑ Physically-isolated Micrologic flip-flop compared to a dime from *LIFE* magazine March 10, 1961

Jay Last leads development of the first commercial IC based on Hoerni's planar process and Noyce's monolithic approach.

In August 1959, Fairchild Semiconductor Director of R&D, Robert Noyce asked co-founder Jay Last to begin development of an integrated circuit based on Hoerni's planar process (**PAGE 20**) and Noyce's patent (**PAGE 21**). After building a multi-chip flip-flop with discrete transistors to demonstrate the concept at Wescon, Last assembled a team including Sam Fok, Isy Haas, Lionel Kattner, and James Nall. Based on characterization data prepared by Don Farina, Robert Norman of the applications department designed a flip-flop with four-transistors and five resistors using a modified Direct Coupled Transistor Logic (DCTL) circuit as most compatible with early planar processing capabilities.

Integrating multiple interconnected devices on one chip posed many new engineering challenges. The first working monolithic devices produced on May 26, 1960 used physical isolation to achieve electrical separation between components. Deep channels were etched from the rear of the silicon wafer and filled with non-conducting epoxy. The preferred production method, *p-n* junction electrical isolation using a boron diffusion technique developed by Haas and Kattner, yielded working circuits on September 27, 1960.

Fairchild presented advanced information at engineering conferences and provided prototype samples to customers in 1960. Under the trade name μLogic (Micrologic), the type "F" flip-flop function was announced to the public in March 1961 via a press conference at the IRE Show in New York and a photograph in *LIFE* magazine. Five additional circuits, including the type "G" gate function (**PAGE 26**), a half adder, and a half shift register, were introduced in October.

Metal Oxide Semiconductor (MOS) transistor demonstrated

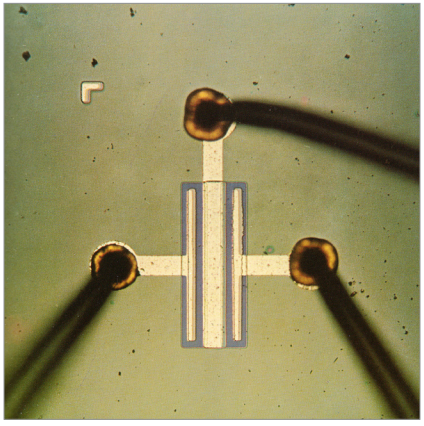
1960

PAGE 23

John Atalla and Dawon Kahng fabricate working transistors and demonstrate the first successful MOS field-effect amplifier.

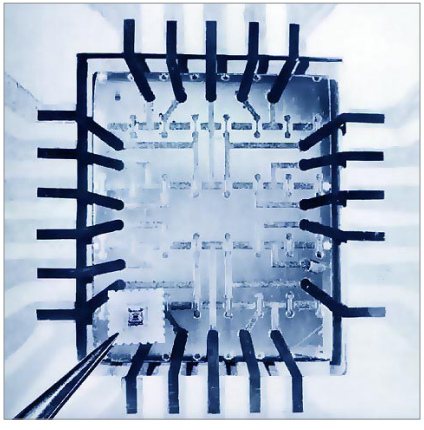
In 1959, M. M. (John) Atalla and Dawon Kahng at Bell Labs achieved the first successful insulated-gate field-effect transistor (FET), which had been long anticipated by Lilienfeld, Heil, Shockley and others (1926 Milestone) by overcoming the "surface states" that blocked electric fields from penetrating into the semiconductor material. Investigating thermally grown silicon-dioxide layers, they found these states could be markedly reduced at the interface between the silicon and its oxide in a sandwich comprising layers of metal (M, gate), oxide (O, insulation), and silicon (S, semiconductor)—thus the name MOSFET, popularly known as MOS. As their device was slow and addressed no pressing needs of the telephone system, it was not pursued further. In a 1961 memo, however, Kahng pointed out its potential "ease of fabrication and the possibility of application in integrated circuits." But researchers at Fairchild and RCA *did* recognize these advantages. In 1960, Karl Zaininger and Charles Meuller fabricated an MOS transistor at RCA and C. T. Sah of Fairchild built an MOS-controlled tetrode. Fred Heiman and Steven Hofstein followed in 1962 with an experimental 16-transistor integrated device at RCA.

The MOS transistor conducting region is either *p*-type (making it a "*p*-channel" device) or *n*-type ("*n*-channel" device) material. The latter are faster than *p*-channel but are more difficult to make. MOS devices hit the commercial market in 1964. General Microelectronics (GME 1004) and Fairchild (FI 100) offered *p*-channel devices for logic and switching applications; RCA introduced an *n*-channel transistor (3N98) for amplifying signals. Because of their smaller size and lower power consumption than bipolar devices, over 99 percent of microchips produced today use MOS transistors. Achieving such ubiquity took decades of effort (PAGE 30).



Fairchild Camera & Instrument Corporation

↑ Fairchild FI 100 p-channel MOS switching transistor



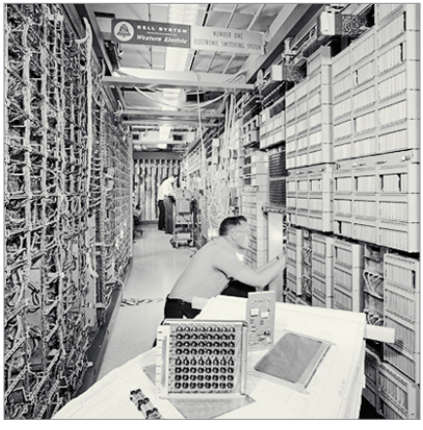
RCA Inc.

↑ RCA 16-transistor MOS integrated circuit held in front of enlarged image

1960

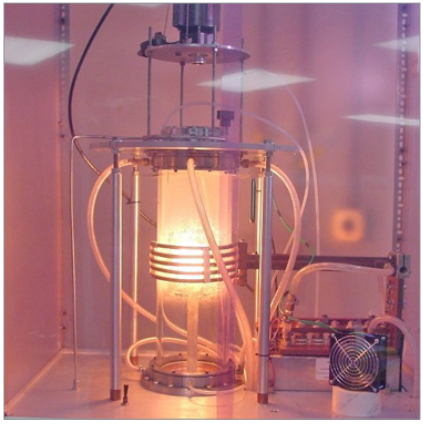
PAGE 24

Epitaxial deposition process enhances transistor performance



AT&T Corporate History

↑ Epitaxial transistors were used in the Bell Number One ESS switch



University of South Carolina

↑ A research-scale epitaxial reactor in operation

Development of thin-film crystal-growth process leads to transistors with high switching speeds.

In 1951, Gordon Teal and Howard Christensen at Bell Labs developed a process, now called epitaxial deposition, to grow a thin layer of material on a substrate that continues the underlying crystalline structure. Sheftal', Kokorish, and Krasilov described similar work on germanium and silicon in the U. S. S. R. in 1957.

At the urging of Ian Ross, a Bell Labs team led by Henry Theurer used chemical-vapor deposition to add a thin epitaxial layer of silicon between the base and collector of a transistor in 1960. This approach raised the transistor's breakdown voltage while dramatically increasing its switching speed (PAGE 25), two important circuit-design characteristics. The added manufacturing cost of the extra process step was more than offset by improvements in device performance. The technology was quickly transferred to Western Electric and used in manufacturing silicon transistors for electronic telephone switching in the Bell System.

Theurer gave a presentation on epitaxial transistors at the June 1960 Solid-State Device Research Conference that aroused widespread interest. Fairchild used epitaxy to fabricate the 2N914, one of its most successful transistors introduced in March 1961 and quickly emulated by Rheem, Sylvania, and Texas Instruments. Motorola applied the process to mass produce devices for automotive alternators. Epitaxial silicon also had an important impact on the manufacturing yield of early bipolar integrated circuits by allowing electrical isolation of the individual circuit components to be accomplished much more easily. It later found widespread application in the manufacture of MOS products. Epitaxial growth techniques are also used to form the ultra-thin layers common in compound-semiconductor manufacturing.

Silicon transistor exceeds germanium speed

1961

PAGE 25

Computer architect Seymour Cray funds development of the first silicon device to meet the performance demands of the world's fastest machine.

Seymour Cray had worked with General Transistor Corporation's germanium transistors at Univac. On founding Control Data Corporation in 1957 with William Norris, Cray asked General Transistor to develop a fast switching germanium device for the CDC 1604 that in 1960 became the first commercially successful large-scale transistor machine for scientific computing.

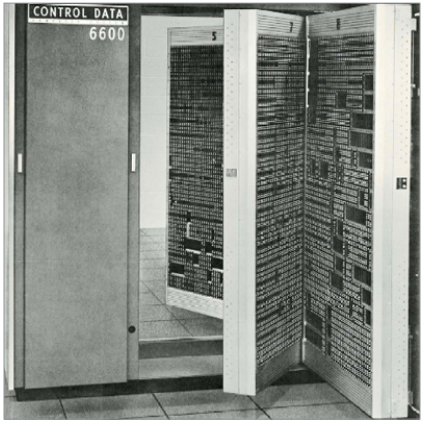
With the goal of building the world's fastest supercomputer, Cray required a transistor that switched in less than 3 nanoseconds while operating in a high temperature environment created by hundreds of thousands of devices operating in close proximity. Early silicon transistors offered superior operation to germanium at elevated temperature but were too slow for many computer designs.

Cray awarded Fairchild Semiconductor a $500,000 development contract to build a new transistor for the CDC 6600. Jean Hoerni met the specification by combining "gold-doping"—the addition of gold impurities—together with the new epitaxial deposition process (PAGE 24). The 2N709 (FT-1310) *n-p-n* device was introduced in July 1961 as the first silicon transistor to exceed germanium speed.

Each CDC 6600 used 600,000 transistors packaged in a unique cordwood-style module configuration to minimize connecting wire lengths. In 1964, the company placed "one of the largest single orders in the history of the semiconductor industry" with Fairchild for over 10 million devices. Scientific Data Systems was another early adopter of high-speed silicon transistors for logic applications in the Sigma series computers.

Fairchild Camera & Instrument Corporation

↑ Jean Hoerni working in the lab



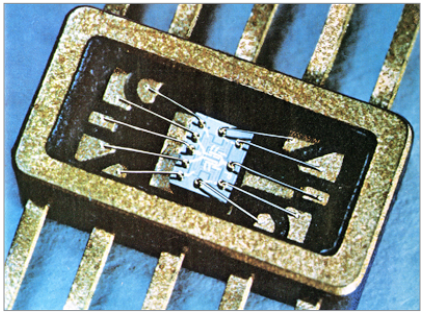
Control Data Corporation

↑ Open logic and memory "leaves" of a CDC 6600

1962

PAGE 26

Aerospace systems are the first applications for ICs in computers



Philco-Ford Microelectronics

↑ Philco Ford also produced the Fairchild Type "G" Micrologic gate for the Apollo Guidance Computer

U. S. National Aeronautics and Space Administration

↑ Apollo logic module assembled by Raytheon

The size, weight, and reduced power consumption of integrated circuits compared to discrete transistor designs justify their higher cost in military and aerospace systems.

The first integrated circuits were relatively slow, replaced only a handful of components, and sold for many times the price of their discrete transistor counterparts. Aerospace and military systems were among the few applications where the low power consumption and small size outweighed these drawbacks. In 1961, Jack Kilby's colleague Harvey Cragon built a demonstration "Molecular Electronic Computer" for the U. S. Air Force to show that 587 TI ICs could replace 8,500 transistors and other components that performed the same function in a conventional design.

Beginning in 1961, Fairchild Micrologic devices (**PAGE 22**) were designed into the AC Spark Plug MAGIC and Martin MARTAC 420 computers but NASA's Apollo Guidance Computer (AGC) was the most significant early project. Designed by MIT in 1962 and built by Raytheon, each system used about 4,000 "Type-G" (3-input NOR gate) circuits. Consuming 200,000 units at $20–30 each, the Apollo Guidance Computer was the largest user of ICs through 1965.

Engineer Bob Cook designed Series 51 DCTL, Texas Instruments' first planar IC family, to meet a low-power specification for the Optical Aspect Computer on NASA's Interplanetary Monitoring Probe (IMP). Using the SN510 and SN514 as binary counters, flip-flops, and inhibiting circuits, the IMP satellite carried the first ICs into orbit in 1963. In 1962, TI won a contract from the Autonetics Division of North American Aviation to design 22 custom circuits for the Minuteman II missile guidance system. Clevite and Westinghouse also developed circuits for the Minuteman project, which by 1965 overtook NASA's Apollo procurement as the largest single consumer of ICs.

Ferranti Semiconductor Ltd. of England developed MicroNOR, one of Europe's first IC logic families, in 1961 to miniaturize on-board computing systems in U. K. Royal Navy systems.

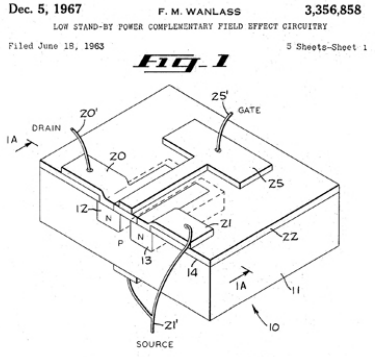
Complementary MOS circuit configuration is invented

Frank Wanlass invents the lowest power logic configuration but performance limitations impede early acceptance of today's dominant manufacturing technology.

In a 1963 conference paper, C. T. Sah and Frank Wanlass of the Fairchild R&D Laboratory showed that logic circuits combining *p*-channel and *n*-channel MOS transistors in a complementary symmetry circuit configuration drew close to zero power in standby mode. Wanlass patented the idea that today is called CMOS.

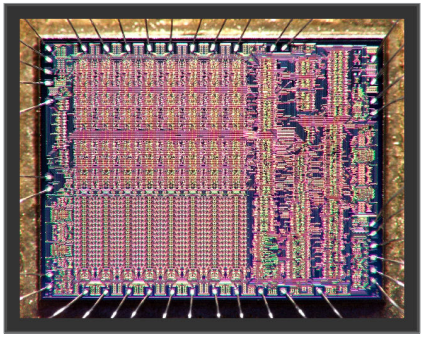
RCA Research Laboratories and the Somerville manufacturing operation pioneered the production of CMOS technology (under the trade name COS/MOS) for very low-power integrated circuits, first in aerospace and later in commercial applications. Gerald Herzog led a major CMOS logic and memory circuit design program for an Air Force computer in 1965. In 1968, the company demonstrated a 288-bit static RAM and introduced the first members of the popular CD4000 family of general-purpose logic devices. Using a unique silicon-gate, closed-geometry CMOS process to minimize leakage, RCA's 1975 COSMAC 1802 microprocessor was the forerunner of millions of engine control processors built for Chrysler automobiles.

The first high-volume applications for CMOS circuits emerged in battery-operated consumer products, such as digital watches and portable instruments, that did not demand the ultimate in speed. By 1978, when Toshiaki Masuhara of Hitachi described a high-speed RAM at ISSCC, the combination of smaller lithography with the silicon-gate process enabled CMOS to compete in performance with bipolar and conventional MOS. As designers took advantage of scaling (PAGE 45) to pack hundreds of thousands of transistors onto a chip, CMOS provided the best solution to manage the resulting power density issues.



U.S. Patent Office

↑ CMOS device structure from Frank Wanlass's patent drawing



William Blair

↑ The RCA COSMAC 1802 CMOS microprocessor die

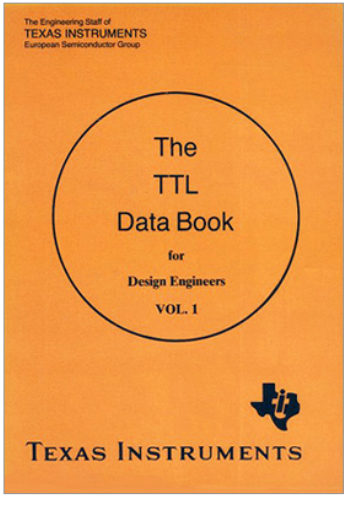
1963

Standard logic IC families introduced

PAGE 28

Fairchild Camera & Instrument Corporation

↑ Dr. Thomas A. Longo developed SUHL TTL at Sylvania in 1963



Texas Instruments, Inc.

↑ The indispensable data manual of the 1970s

Diode Transistor Logic (DTL) families create a high-volume market for digital ICs but speed, cost, and density advantages establish Transistor Transistor Logic (TTL) as the most popular standard logic configuration by the late 1960s.

Integrated versions of discrete diode transistor logic (DTL) circuits became the first high-volume IC product lines. Designed by Orville Baker in 1962, the Signetics SE100 Series DTL family was overtaken in 1964 by the better noise immunity and lower cost of Fairchild's 930 Series establishing a competitive industry leap-frog pattern that continues today.

Patented by James Buie of Pacific Semiconductor in 1961, TTL (Transistor Transistor Logic) emerged as the most popular logic configuration of the next two decades. Unaware of Buie's work but inspired by an "all transistor" logic circuit described by Ruegg and Beeson of Fairchild, Thomas Longo led the design of the first TTL family, Sylvania Universal High-level Logic (SUHL) in 1963. Encouraged by SUHL's success in winning a high-profile Hughes military design (the Phoenix missile), TI introduced the competing SN5400 Series TTL family the following year. The company announced the SN7400 Series in low cost plastic packages for industrial customers in 1966 and quickly gained a greater than 50% share of the logic market.

By 1968, lithography advances significantly increased the number of transistors that could be integrated on a chip. Eager to win a share of the TTL business, Fairchild (9300 Series) and Signetics (8200 Series) pioneered the design of TTL-MSI (Medium Scale Integration—up to 100 logic gates per chip) functions such as counters, shift registers, and arithmetic logic units. Many vendors applied Schottky (PAGE 40) and CMOS (PAGE 27) technology to build larger, faster, and lower power TTL-compatible functions that extended the useful life and range of applications of this popular logic configuration.

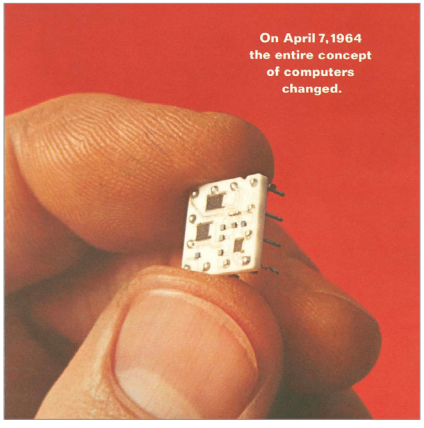
Hybrid microcircuits reach peak production volumes

Multi-chip SLT packaging technology developed for the IBM System/360 computer family enters mass production.

In the late 1950s, the U. S. Army Signal Corps. program, with RCA as prime contractor, developed hybrid microcircuits as dense micro-module assemblies of electronic components. Hybrid circuits comprise one or more transistor chips and passive components mounted on ceramic substrates and interconnected with wires or conductive traces. After the introduction of monolithic ICs, functions that required high-density packaging and that could not be integrated for economic or technical reasons continued to be manufactured as hybrids. Examples include precision analog devices, automotive controls, and early semiconductor memories.

IBM developed Solid Logic Technology (SLT) for the System/360 computer family in 1964 prior to the ability of monolithic ICs to meet the cost and speed demands of large computers. Transistor chips and passive components mounted on 0.5" square ceramic modules with vertical pins consumed less power and space while offering faster speed and superior reliability compared to printed-circuit boards with packaged transistors. IBM produced hundreds of millions of SLT modules in a highly-automated, specially-built plant in East Fishkill, NY. Bell Laboratories used Beam Lead Sealed-Junction (BLSJ) devices and thin-film interconnects to produce hybrid ICs for telephone systems through the late-1960s.

Early hand-crafted hybrid circuits were labor intensive and expensive to produce but are now widely used in applications where integrated devices cannot meet specific objectives. Multichip modules (MCM) and packages (MCP) are modern machine-assembled hybrid circuits, used for certain high-performance microprocessor and memory applications, automotive systems, and RF transceivers in cell phones and wireless LANs.



International Business Machines Corporation

↑ A 1964 IBM System/360 brochure cover featuring an SLT module

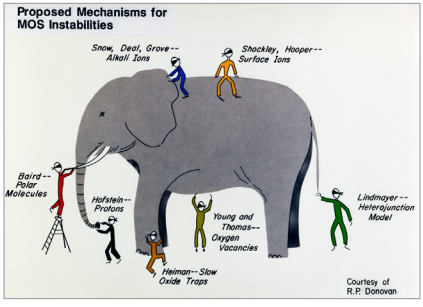
International Business Machines Corporation

↑ Typical IBM System/360 computer center installation

1964

PAGE 30

First commercial MOS IC introduced



Bruce Deal and Harry Sello

↑ R. P. Donovan's illustration of the spectrum of MOS instability explanations presented at a 1966 symposium

Fairchild Camera & Instrument Corporation

↑ Andy Grove, Bruce Deal, and Ed Snow discuss MOS technology at the Fairchild Palo Alto R&D laboratory in 1966

General Microelectronics uses a Metal-Oxide-Semiconductor (MOS) process to pack more transistors on a chip than bipolar ICs and builds the first calculator chip set using the technology.

Achieving the MOS promise of higher density and lower cost than bipolar (**PAGE 23**) proved more difficult than anticipated due to complex manufacturing and reliability issues. Speakers at a symposium on the Physics of Failure in Electronics likened competing solutions to the story of the blind man and the elephant—it depends on which part you examine. Frederic Heiman and Steven Hofstein built an experimental 16-transistor IC at RCA in 1961 and later made important contributions to understanding surface oxide quality. Between 1963 and 1966, Bruce Deal, Andrew Grove, and Ed Snow at Fairchild identified the issue of sodium contamination and published many papers on the electrical nature of oxides that informed Grove's classic textbook Physics and Technology of Semiconductor Devices. Collaboration and competition across the globe, including researchers from NEC, IBM and Philips, resolved the fundamental yield and reliability issues by the end of the decade that allowed MOS to emerge as the dominant IC technology.

General Microelectronics introduced the first commercial MOS integrated circuit in 1964 when Robert Norman used a 2-phase clock scheme to design a 20-bit shift register using 120 *p*-channel transistors. To fund an ambitious 23 custom IC project for the first MOS-based electronic calculator for Victor Comptometer, GMe sold the company to Philco-Ford. When the operation was transferred to Philadelphia most employees moved on to other companies, including AMI and General Instrument, where they continued to develop calculator chips for a burgeoning new market. By 1969, Rockwell Microelectronics had reduced the chip count to four devices for Sharp's first portable machine, the microCompet QT-8D, and went on to become the largest supplier of calculator chips in the early 1970s. Mostek and TI (**PAGE 44**) introduced single-chip (except for external display drivers) solutions in 1971.

The first widely-used analog integrated circuit is introduced

1964

PAGE 31

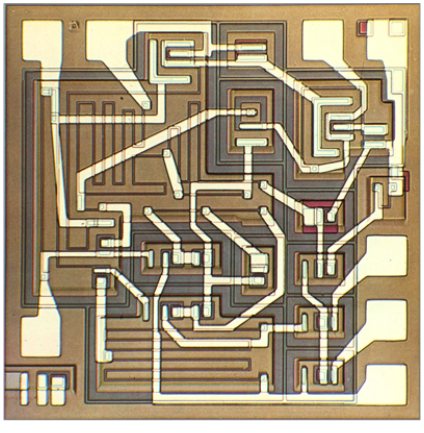
David Talbert and Robert Widlar at Fairchild kick-start a major industry sector by creating commercially successful ICs for analog applications.

Analog, also called linear, circuits amplify and condition signals from continually varying phenomena such as sound, temperature, and radio waves. Because of the nearly infinite resolution required to process these signals, analog circuits demand high precision in design and manufacturing. Early analog circuit designs were paced by the operational amplifier (op-amp) concepts developed by Columbia University researcher Loebe Julie. George Philbrick exploited these in his vacuum tube K2-W op-amp for performing electronic signal integration in 1952. The first germanium transistor op-amp appeared in 1958 with silicon versions in 1960. Nexus Research Labs offered the first pre-configured op-amp modules in 1962 followed shortly by Burr-Brown and Philbrick Researches.

Amelco, Fairchild, RCA, TI, and Westinghouse—where H. C. Lin conceived the idea of on-chip component matching—developed early monolithic amplifiers. But the Fairchild μA702 op amp, created in 1964 by the team of process engineer Dave Talbert and designer Robert Widlar, was the first widely-used device. Their 1965 successor, the μA709, established a mass market for analog ICs. Talbert and Widlar moved to Molectro (later acquired by National) in late 1965 where they built a linear dynasty beginning with the LM101. Then in 1968, Dave Fullagar of Fairchild one-upped the LM101 by adding an internal compensating capacitor to deliver the μA741, the most popular op-amp of all time. Analog Devices' designers followed the basic 741 architecture for its first high-precision op-amp in 1971. Specialty analog IC manufacturers evolved extensive catalogs of amplifiers, comparators, data converters, power management devices, and numerous specialty circuits for automotive, consumer and communications applications.

National Semiconductor

↑ Robert Widlar inspects the LM10 mask layout circa 1977



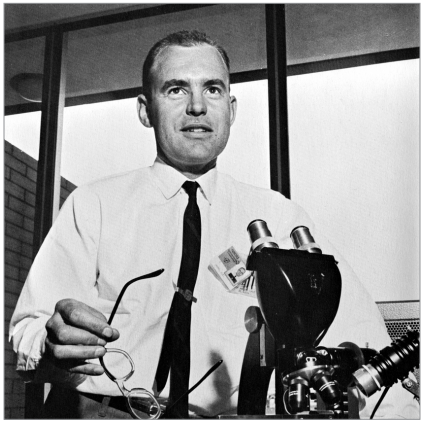
Fairchild Camera & Instrument Corporation

↑ Talbert and Widlar's μA709 high-performance operational amplifier (1965)

1965

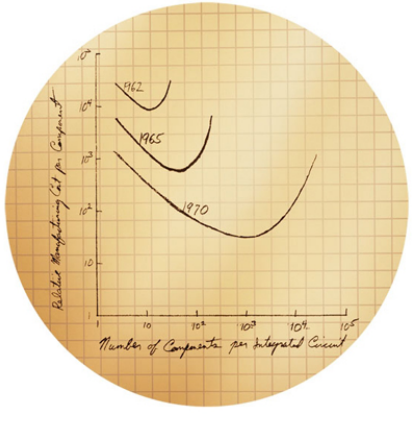
PAGE 32

"Moore's Law" predicts the future of integrated circuits



Fairchild Camera & Instrument Corporation

↑ Gordon Moore at Fairchild R&D in 1962



Fairchild Camera & Instrument Corporation

↑ Cost vs. time sketch from Moore's 1964 notebook

Fairchild's Director of R&D predicts the rate of increase of transistor density on an integrated circuit and establishes a yardstick for technology progress.

Gordon Moore, Fairchild Semiconductor's Director of R&D, wrote an internal paper in which he drew a line through five points representing the number of components per integrated circuit for minimum cost per component developed between 1959 and 1964. "The Future of Integrated Electronics" attempted to predict "the development of integrated electronics for perhaps the next ten years." Extrapolating the trend to 1975 he projected that the number of components per chip would reach 65,000; a doubling every 12 months. Edited for publication as a magazine article, "Cramming more components onto integrated circuits" was published in *Electronics* on April 19, 1965.

At the 1975 IEEE International Electron Devices Meeting, Moore, by now with Intel, noted that advances in photolithography, wafer size, process technology, and "circuit and device cleverness," especially in semiconductor memory arrays, had allowed his projection to be realized. Adding more recent data, that included a higher mix of microprocessor designs that were somewhat less dense than memories, he slowed the future rate of increase in complexity to "a doubling every two years, rather than every year."

This prediction became a self-fulfilling prophecy that emerged as one of the driving principles of the semiconductor industry. Technologists were challenged with delivering annual breakthroughs that ensured compliance with "Moore's Law," as it was dubbed by Carver Mead. On reviewing the status of the industry again in 1995 (at which time an Intel Pentium microprocessor held nearly 5 million transistors) Moore concluded that "The current prediction is that this is not going to stop soon." Devices exceeding one (U. S.) billion transistors exist today.

Large computers demand specialty integrated circuits

1965

PAGE 33

Burroughs and RCA announce the first mainframe computer families based on monolithic integrated circuit technology.

Large electronic data processing systems for business and scientific applications are called "mainframe" computers. In the 1960s, mainframe vendors distinguished their systems in the marketplace through proprietary hardware, operating systems, and applications software. They demanded components offering unique features and significantly faster speed (PAGE 25) than general-purpose logic solutions (PAGE 28). As mainframe systems offered the highest production volume business opportunities, teams of engineers at Fairchild, Motorola, Signetics, TI, and others handcrafted families of custom and special ICs for these customers.

Two of the earliest mainframe designs to use monolithic ICs were the RCA Spectra 70 series (1965) and the Burroughs B2500/3500 (1966) machines. RCA developed Current Mode Logic (CML) circuits internally and worked with IC vendors to manufacture them. Burroughs engineers cooperated with Robert Seeds at Fairchild to develop a Complementary Transistor Logic (CTL) family that also powered Hewlett-Packard's 3000 Series. IBM produced the majority of its needs in-house while CDC, General Electric, Honeywell, NCR, SDS, and Univac contracted for custom design services.

In 1962, Jan Narud led the development of Motorola's MECL (Motorola Emitter Coupled Logic) family, a monolithic implementation of IBM's transistor-based very high speed logic circuits. Although offered as standard products, expensive multi-layer p.c. boards and system cooling requirements limited ECL usage largely to high-performance scientific computer applications at Control Data Corporation, Cray, GE, Hitachi, ICL, and others. In 1976, each Cray 1 machine consumed 250,000 dual F100K ECL gate packages from Fairchild that offered switching times of under 1ns per gate.

Fairchild Camera & Instrument Corporation

↑ A handbook describing how to specify a custom IC from Fairchild

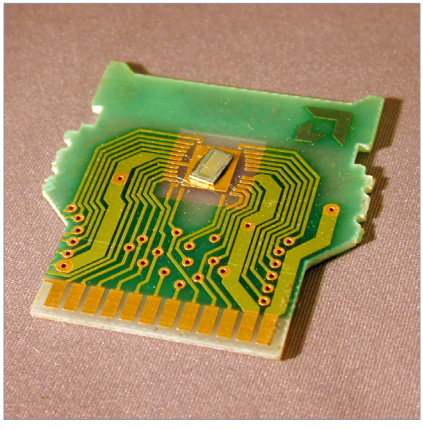
Burroughs Corporation

↑ Burroughs B25/3500 Series used CTL ICs from Fairchild & ITT

1965

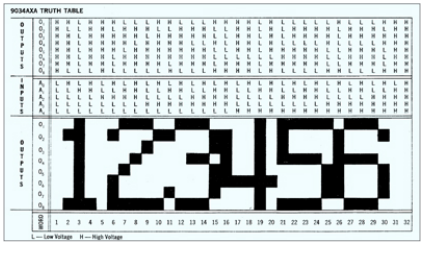
PAGE 34

Read-Only Memory is the first dedicated IC memory configuration



CHM Dan Rose Packaging Collection. Gift of SEMI

↑ Atari video game cartridge board with AMD 4K-bit MOS ROM circa 1982



Fairchild Camera & Instrument Corporation

↑ 256-bit ROM number generator programming table

Factory-programmable read-only memories (ROMs) generate the first integrated circuit random access memory applications.

As data is permanently written into a Read-Only Memory during the manufacturing process, ROM storage is used for information that will remain unchanged throughout the life of a system, such as microprogram code, look-up tables, character generation, etc. Semiconductor ROMs are built from discrete or integrated arrays of diodes placed between signal wires organized in rows and columns. During wafer fabrication of integrated ROMs the last masking step makes connection to diodes specified by the customer. As a diode represents the smallest possible memory cell structure, ROM devices offer the highest density form of semiconductor memory.

In 1965, Sylvania produced a 256-bit bipolar TTL ROM for Honeywell that was programmed one bit at a time by a skilled technician at the factory who physically scratched metal link connections to selected diodes. Production orders were satisfied with custom-mask programmed devices. The same year, General Microelectronics developed slower but four-times larger 1024-bit ROMs using MOS technology. By the early 1970s, Fairchild, Intel, Motorola, Signetics, and TI offered 1024-bit TTL ROMs, while AMD, AMI, Electronic Arrays, General Instrument, National, Rockwell and others produced 4096-bit (4K) MOS devices.

Desktop calculator consumption, the first high-volume application, was surpassed by video game cartridges that used hundreds of millions of 16K and larger devices from U. S. and Japanese vendors. Production of Nintendo's first Super Mario Brothers NES game alone exceeded 40M units. As each ROM is manufactured to order, customers were often frustrated with long delivery times and vendors overwhelmed by production logistics. Relief came in the form of user-programmable ROMs (PROMs) (PAGE 42).

Semiconductor RAMs developed for high-speed storage

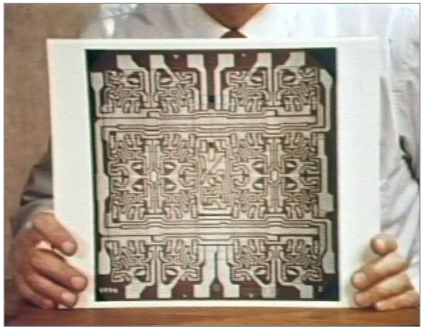
1966

PAGE 35

Sixteen-bit bipolar devices are the first ICs designed specifically for high speed read/write memory applications.

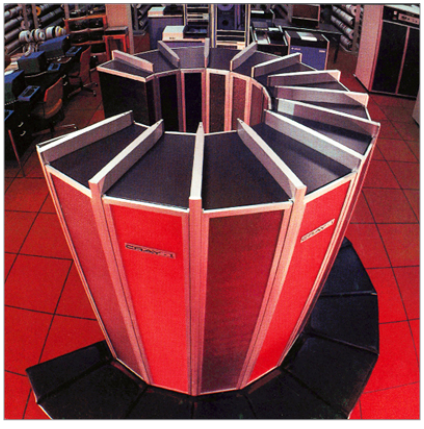
Random Access Read-Write Memories (RAMs) store information that changes frequently and must be accessed quickly. Offering the lowest cost per storage bit, magnetic ferrite core arrays comprised the dominant RAM technology through the mid-1970s. Operations requiring faster access stored data temporarily in semiconductor flip-flop circuits called registers. IBM Components Division engineers Ben Agusta and Paul Castrucci developed the SP95 16-bit bipolar RAM for the System/360 Model 95 in late 1965. In 1966, a team led by Tom Longo at Transitron built the TMC3162 16-bit TTL scratchpad memory for the Honeywell Model 4200 minicomputer. Fairchild (9033), Sylvania (SM-80), and TI (SN7481) alternated-sourced the design. IBM produced a 64-bit chip for a cache memory in 1966. Fairchild (9035 and 93403), Intel (3101), TI (SN7489) followed with high-speed 64-bit devices as standard products.

In 1969, the IBM East Fishkill, NY facility produced a 128-bit device for the 1971 shipment of System/360 Model 145, the company's first commercial computer to employ semiconductor main memory. Using the 4100 (aka 93400) 256-bit TTL chip designed by H. T. Chua, Fairchild delivered semiconductor main memory systems for the Burroughs Illiac IV computer in April 1970. Using Douglas Peltzer's Isoplanar oxide-isolated process that improved speed while consuming less silicon area, Fairchild's Bill Herndon designed a fast 256-bit TTL memory (93410) in 1971. The Cray 1 supercomputer, introduced in 1976, used 65,000 Fairchild 1024-bit ECL RAM chips (10415) based on the Isoplanar process. Bipolar technology enabled faster computers but it took the MOS process to deliver low-cost solutions for widespread use in main memory and general-purpose applications (PAGE 41).



Fairchild Camera & Instrument Corporation

↑ Metal mask plot for a 16-bit bipolar TTL RAM. Screen image from a 1967 TV documentary



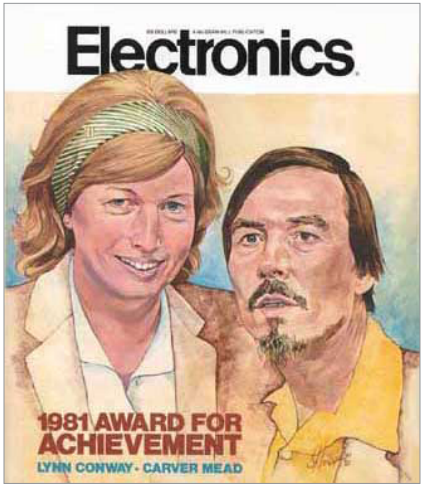
Cray Research

↑ The Cray 1 supercomputer used 65,000 Fairchild 10415 high-speed 1024-bit ECL chips for main memory

1966

PAGE 36

Computer-Aided Design tools developed for ICs



McGraw Hill Publications

↑ 1981 Electronics Award for Achievement to Conway and Mead

Fairchild Camera & Instrument Corporation

↑ IBM 360/67 mainframe-powered CAD system at Fairchild in 1967

IBM engineers pioneer computer-aided electronic design automation tools for reducing errors and speeding design time.

As ICs began to incorporate hundreds of gates and thousands of transistors, the computers they enabled were harnessed to speed the design task and eliminate errors. This process is called CAD (Computer-Aided Design) or EDA (Electronic Design Automation). IBM pioneered EDA in the late 1950s with documentation of the 700 series computers. By 1966, James Koford and his colleagues at IBM Fishkill were capturing SLT hybrid circuit module (**PAGE 29**) designs on graphical displays, checking them for errors and automatically converting the information into mask patterns. After Koford joined Fairchild R&D he worked with Hugh Mays, Ed Jones, and others to apply this process to monolithic ICs. Their efforts created logic simulators (FAIRSIM), test program generators, and place and route software for gate arrays and standard cells (**PAGE 37**) that laid the ground work for generations of EDA tools.

Two important EDA projects originated outside the mainstream of the industry. Larry Nagel and Donald Pederson, with later contributions by Richard Newton, at U.C. Berkeley developed the SPICE (Simulation Program with IC Emphasis) circuit simulation program in the 1960s. A new methodology described in the 1979 Introduction to VLSI Systems by Lynn Conway of Xerox, PARC and Carver Mead of California Institute of Technology demystified the process of chip design for system designers.

Commercial logic synthesis packages from Cadence and Synopsys in the 1980s were stimulated by research at U.C. Berkeley (SIS), U.C.L.A. (RASP), and University of Colorado, Boulder (BOLD). These, together with advancements in place and route, logic simulation, and design rule verification from other vendors, allowed IC design productivity to keep pace with increasing device complexity.

Application-specific integrated circuits employ Computer-Aided Design

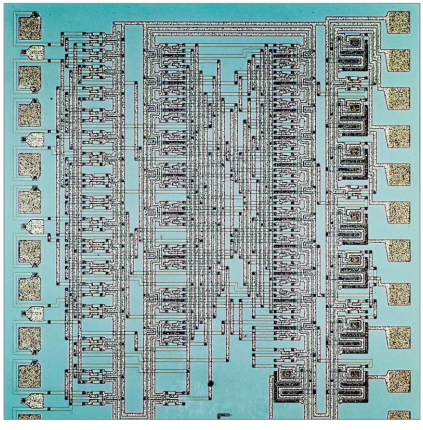
1967

PAGE 37

Automated design tools reduce the development engineering time to design and deliver complex custom integrated circuits.

As ICs increased in complexity their design and manufacturing turn-around times stretched out to years even as some end product life cycles shrank to a single season. To speed the availability of prototype quantities of complex custom circuits for the Air Force in 1967 IBM and Texas Instruments developed "discretionary-wiring" approaches that employed a unique computer-generated (PAGE 36) metal mask for every wafer.

Two approaches developed for volume production of custom designs are gate arrays and standard cells—collectively known as Application-Specific ICs (ASIC). Gate arrays are produced as wafers of unconnected transistors. As the customizing interconnections are applied at the final manufacturing step, although less efficient in silicon usage than handcrafted chips, prototypes can be produced in days rather than months. Early gate array suppliers such as Ferranti/Interdesign designed the custom connections manually. In 1967, Fairchild introduced the Micromatrix family of bipolar DTL and TTL arrays that used CAD tools to perform this operation interactively. Robert Lipp designed the first CMOS array for International Microcircuits in 1974 but viable CAD support was not forthcoming for several years. Standard cell ICs employ a full set of fabrication masks using designs assembled from catalog functions stored in a computer library. They offer a compromise between silicon-efficient handcrafted designs and the fast turn-around of gate arrays. Fairchild and Motorola offered early MOS standard cell capabilities under the trade names Micromosaic and Polycell. VLSI Technology (founded 1979) and LSI Logic (1981) successfully exploited these CAD-based ASIC concepts abandoned by the original vendors in early 1970s largely due to the then high cost of computing time.



Fairchild Camera & Instrument Corporation

↑ Micromosaic – a 1968 standard cell design for GE Avionics. One of the industry's first designs for revenue

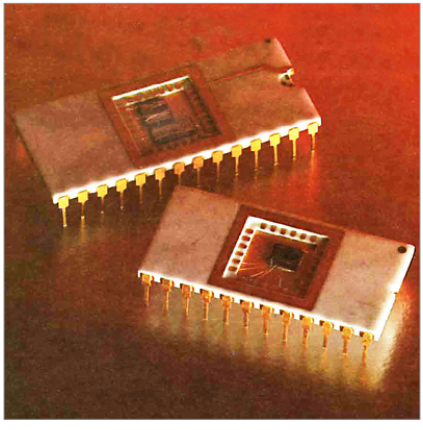
Sinclair Research

↑ A Ferranti ULA (Uncommitted Logic Array) integrated 14 TTL IC packages for the Sinclair ZX81 PC in 1981

1968

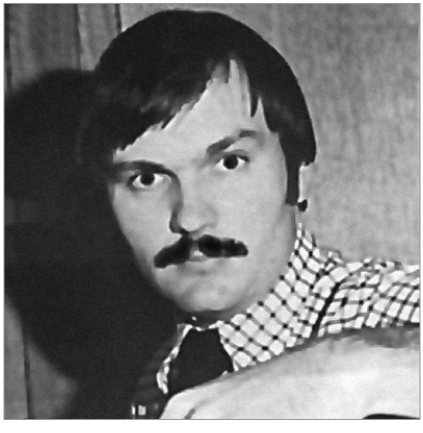
PAGE 38

Dedicated current source IC integrates a data conversion function



Analog Devices, Inc.

↑ Separate bipolar and CMOS packages comprise a 12-bit ADC (AD574) from 1978



Analog Devices, Inc.

↑ Peter Holloway designed both the AD 561 and 574

The precision manufacturing requirements of combining analog and digital capability on one chip made them one of the last product areas to yield to monolithic solutions.

Digital is the most efficient form for manipulating many kinds of information. However, real world data is analog in nature and must be converted to digital form for processing. Integrated circuits incorporating analog and digital circuitry where signals are translated between these two modes are called mixed-signal devices. Numerous approaches are used to accomplish Analog to Digital (ADC) and Digital to Analog (DAC) conversion; each entails different trade offs between accuracy, speed, and cost.

Fairchild's George Erdi designed one of the first ICs dedicated to data conversion applications, the μA722 10-bit Current Source, in 1968. In the 1970s, many vendors including Analog Devices, AMD, Harris, Intersil, Motorola, National Semiconductor, Precision Monolithics (PMI), TI, and TRW developed families of devices that integrated specific portions of the data conversion function.

Using diffused resistors PMI's Dan Dooley designed the first fully integrated DAC, the 6-bit DAC01 in 1969. Motorola (MC1408) and PMI (DAC08) followed with 8-bit devices in 1975. The accuracy of data converters, expressed as bit resolution, is limited by the accuracy of a string of resistors. The larger the bit resolution, the higher the accuracy required of the resistors. In 1976, Peter Holloway at Analog Devices laser trimmed thin-film resistors on the wafers to achieve the required precision for the first single-chip 10-bit DAC, the AD561. Using integrated injection logic (I2L) bipolar circuit techniques, Paul Brokaw of Analog Devices designed the first monolithic ADC, the 10-bit AD571, in 1978. As ADCs require more circuit components than DACs, two-chip bipolar and CMOS solutions prevailed for 12-bit and higher functions through the early 1980s.

Silicon gate technology developed for ICs

1968

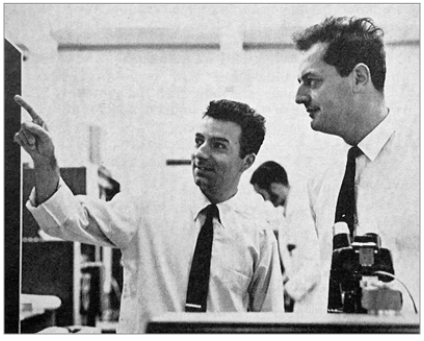
PAGE 39

Federico Faggin and Tom Klein improve the reliability, packing density, and speed of MOS ICs with a silicon-gate structure. Faggin designs the first commercial silicon-gate IC—the Fairchild 3708.

Robert Kerwin, Donald Klein and John Sarace at Bell Labs improved the speed, reliability, and packing density of MOS transistors (**PAGE 23**) by replacing the aluminum metal gate electrode with a polycrystalline layer of silicon in 1967. Boyd Watkins described a similar self-aligned, silicon-gate structure at General Microelectronics in 1965 but patent filing was delayed until 1969. As project leader, Federico Faggin worked with Tom Klein at Fairchild R&D to commercialize the technology for ICs. Faggin then redesigned an existing *p*-channel metal-gate 8-channel analog multiplexer circuit using the new technology and in 1968 Fairchild introduced the first silicon-gate IC, the 3708.

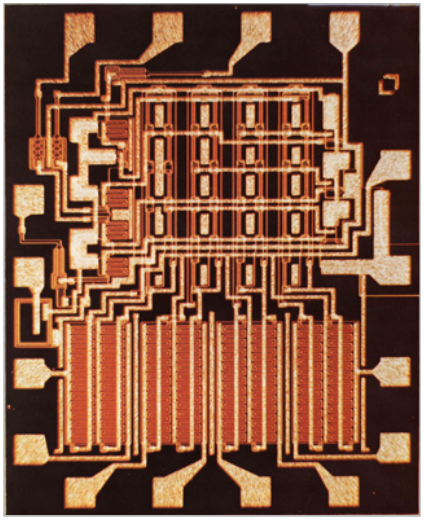
Following Fairchild's proof of concept, Intel pursued silicon-gate as the primary technology for semiconductor memories as it delivered 3 to 5 times faster speed in half the chip area of conventional MOS. Intel's first commercial MOS device, the 1101 256-bit RAM, was introduced in 1969. Faggin joined Intel in 1970. By adding a buried contact and other process enhancements for logic applications he was able to design the 4004 microprocessor CPU to fit on a manufacturable die size (**PAGE 43**).

Intel's pioneering work in transferring silicon-gate to production presented many challenges but gave the company a significant competitive lead by permitting the early introduction of high density dynamic RAMs (**PAGE 41**). It also enabled the development of EPROM memories (**PAGE 42**) that could not be accomplished economically with metal gate technology. Within five years silicon-gate MOS had become the industry standard process for new IC product development replacing bipolar technology in all but the highest speed applications.



Fairchild Camera & Instrument Corporation

↑ Federico Faggin and Tom Klein at Fairchild R&D in 1967



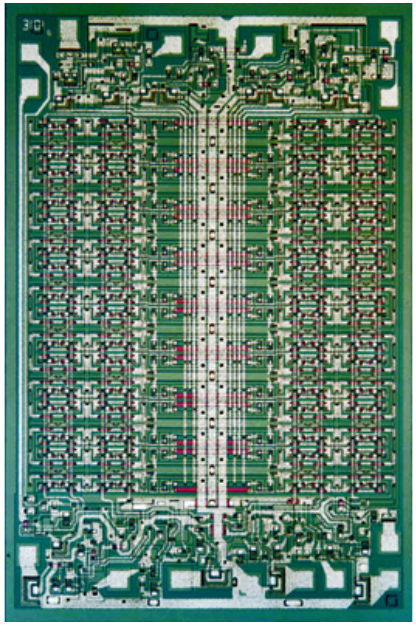
Fairchild Camera & Instrument Corporation

↑ Fairchild 3708, the first commercial silicon-gate IC designed by Federico Faggin in 1968

1969

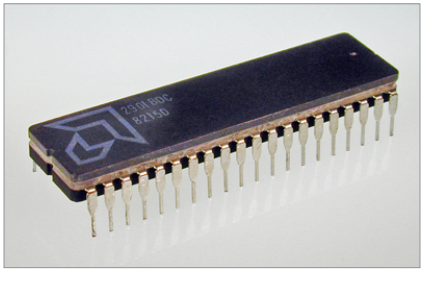
PAGE 40

Schottky-barrier diode doubles the speed of TTL memory & logic



Intel Corporation

↑ The i3101 Schottky TTL 64-bit RAM was Intel's first product



Advanced Micro Devices, Inc.

↑ Introduced in 1975, the Am2901 bit-slice microprocessor used Low-power Schottky (LS) process technology.

Design innovation enhances speed and lowers power consumption of the industry standard 64-bit TTL RAM architecture, and is quickly applied to new bipolar logic and memory designs.

Since 1963, TTL (**PAGE 28**) device complexity had advanced twenty-fold but switching speeds remained relatively unchanged at delays of 10-15 ns per gate. Speed is determined by how quickly charge stored in a transistor can be removed. Gold-doping (**PAGE 25**) improved this but was difficult to control. In 1964, J. R. Baird of Texas Instruments (TI) proposed using a metal-semiconductor diode, called a Schottky-barrier diode, to shunt charge around the transistor. Ted Jenkins and Garth Wilson of Fairchild fabricated such a diode on a bipolar integrated circuit in 1967. Concurrently Japan's Electrotechnical Laboratory developed a similar design. Jenkins later used a Schottky diode in the design of Intel's first product, the i3101 64-bit TTL compatible RAM. Introduced in 1969, the device was nearly twice as fast as earlier TTL products (**PAGE 35**).

In 1971, TI introduced the 74S Series TTL logic family using Schottky diodes to achieve 3 ns gate delays for high-speed applications. Low-power Schottky versions, designated LS, quickly replaced the original 7400 devices by offering the same speed at one fifth the power consumption. Chairman Mark Shepherd described 7400LS as "the single most profitable product line in the history of Texas Instruments." AMD, Fairchild, Motorola, National, and Signetics also entered the market. Later generations, including Fairchild Advanced Schottky Technology (FAST), combined Schottky diodes with oxide-isolation processes for sub-2ns delays.

In the mid-1970s, micro-programmable "bit-slice" processor families from AMD, Intel, MMI, and Signetics used Schottky technology to integrate LSI building blocks for very high performance arithmetic processing applications.

MOS dynamic RAM competes with magnetic core memory on price

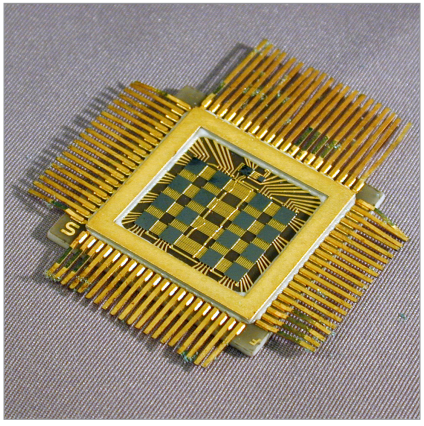
PAGE 41

The Intel i1103 Dynamic RAM (DRAM) presents the first significant semiconductor challenge to magnetic cores as the primary form of computer memory.

John Schmidt designed a 64-bit MOS *p*-channel Static RAM at Fairchild in 1964. Fairchild's 1968 SAM (Semiconductor Active Memory) program for Burroughs assembled sixteen of these chips on ceramic substrates to form 1024-bit hybrid arrays. Monolithic solutions soon overtook this and similar multi-chip projects at Computer Microtechnology, Intel, Motorola, and TI (SMA 2001).

To reduce chip size, Joel Karp of GMe conceived a dynamic clocking scheme that Lee Boysel adapted to build 256-bit dynamic RAMs at Fairchild in 1968 and 1024 and 2048-bit devices at Four Phase Systems in 1969. These and competing DRAMs from Advanced Memory Systems (AMS6001) employed 4 to 6 transistors per bit. Honeywell's Bill Regitz proposed a 3-transistor cell that was implemented by Karp in Intel's *p*-channel silicon gate process (PAGE 39). Improvements suggested by Ted Hoff, designed by Bob Abbott and debugged by Bob Reed resulted in the 1103. Offering much faster speed and priced at 1 cent/bit, beginning in 1970 the 1103 quickly replaced magnetic core technology for computer main memory. Walter Krolikowski of Cogar described an even faster *n*-channel DRAM in 1970. IBM was the first manufacturer to commit to this new process technology on System 370/158 in 1972.

Mostek's Robert Proebsting used ion-implanted resistors to reduce power consumption and die size sufficiently to pack 4K bits (MK4096) into a conventional 16-pin package in 1973. At the 16K level (MK4116) in 1976 Mostek adopted the single transistor memory cell patented by IBM researcher Robert Dennard and design methods described by Karl-Ulrich Stein of Siemens. This approach led to 64K DRAMs from Japanese and U. S. vendors before the end of the decade and large capacity semiconductor memory systems that were as reliable as and more economical than magnetic cores.



Fairchild Camera & Instrument Corporation

↑ Fairchild 1024-bit SAM multi-chip memory plane uses sixteen 64-bit PMOS Static RAM chips (1968)

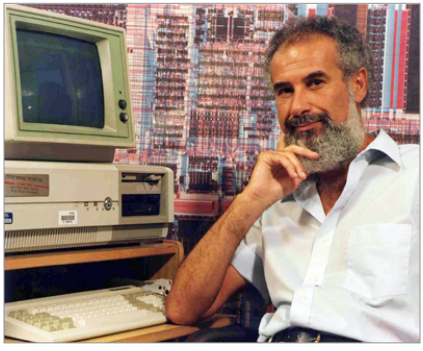
Intel Corporation

↑ "Cores Lose Price War": With this advertisement for the 1103 DRAM, Intel aggressively pursued the challenge of replacing magnetic core memory in computer main memory applications

1971

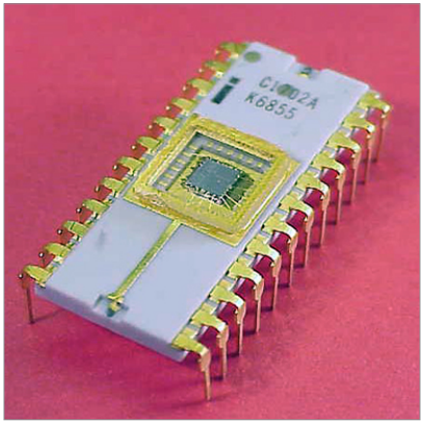
PAGE 42

Reusable programmable ROM introduces iterative design flexibility



Intel Corporation

↑ EPROM inventor Dov Frohman with mask design drawings



Intel Corporation

↑ A quartz window admits UV light for EPROM data erasure

Dov Froman's ultra-violet light erasable ROM design offers an important design tool for the rapid development of microprocessor-based systems, called an erasable, programmable read-only-memory or EPROM.

A masked ROM (**PAGE 34**) pattern is created in the factory and thus takes several weeks to produce each design iteration. User-programmable ROM (PROM) devices allow the designer to make changes in the lab. Radiation Inc. introduced a 512-bit bipolar TTL PROM (64×8) with metal fuse links connected to each bit in May 1970. A user "burned" the one-time-programmable fuses on programming units from Data I/O, Spectrum Dynamics, and others. Harris (successor to Radiation), Monolithic Memories, Motorola, and Signetics developed 1K through 16K-bit nickel-chromium fuse PROMs. AMD, Intel, and TI entered the market using alternative fuse materials and Schottky technology (**PAGE 40**).

Researchers at Bell Labs and Sperry Rand independently described alterable memory cells that stored charge in the MOS gate dielectric in 1967. At Intel in 1971, Dov Frohman used a floating (unconnected) gate for storage in the 1702 Erasable PROM (EPROM). The 2048-bits of memory could be changed and reused multiple times. The pattern was erased by exposure to ultra-violet light through a quartz window in the package. While much slower performing than bipolar devices, re-usable EPROMs found numerous applications in prototyping ROM codes for microprocessors (**PAGE 43**) and microcontrollers (**PAGE 44**). Intel went on to produce generations of EPROMs up to multi-million bits in density. In 1978, George Perlegos designed the Intel 2816, an Electrically Erasable PROM that eliminated the lengthy UV exposure cycle. On founding Seeq with other Intel employees in 1981, Perlegos developed an improved version that could be programmed and erased in-situ, in the system. Flash, today's most widely used non-volatile memory (NVM) form, was developed in 1984 by Fujio Masuoka of Toshiba and commercialized by Intel in 1988.

Microprocessor condenses CPU function onto a single chip

1971

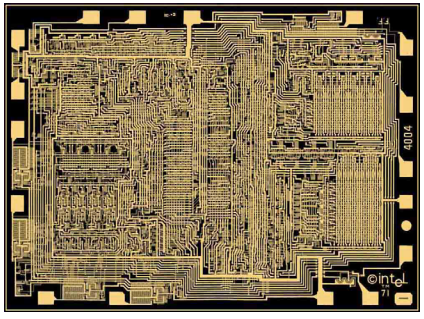
PAGE 43

Intel engineers, led by Federico Faggin, implement Ted Hoff's architectural concept to create the first single-chip computer central processing unit (CPU), now called a micro-processor unit or MPU, to be sold as a standard catalog product.

By the late 1960s, designers were striving to integrate the central processing unit functions of a computer onto a handful of MOS LSI chips. Building on an 8-bit arithmetic logic unit (3800) he designed at Fairchild, in 1969 Lee Boysel created the AL-1, an 8-bit computer processor slice, at Four-Phase Systems Inc. In 1970, Steve Geller and Ray Holt of Garrett AiResearch designed the MP944 chip set to implement the F-14A Central Air Data Computer on six metal-gate chips fabricated by AMI.

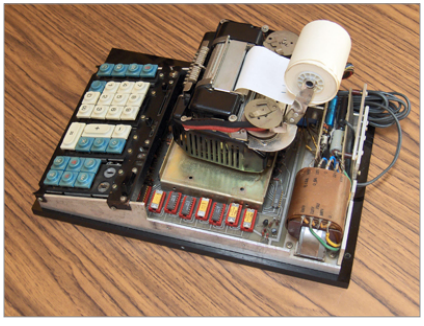
Intel's first microprocessor unit (MPU), as these CPU functions on a chip became known, was conceived by Ted Hoff and Stanley Mazor in 1971. Assisted by Hal Feeney and Masatoshi Shima, Federico Faggin used silicon gate MOS technology (**PAGE 39**) to squeeze the 2300-transistors of the 4004, 4-bit MPU, into a 16-pin package. Faggin also led development of the 8-bit 8008 device announced by Intel in 1972. Designed for CTC (later Datapoint), prototypes of the 8008 function were also built by Texas Instruments as the TMX1795 but never offered commercially. Second generation 8-bit designs from Intel (8080) and from a team led by Tom Bennett at Motorola (6800) in 1974 established widespread acceptance of the MPU concept. A low-cost 6800 clone by MOS Technology (6502) enabled personal computers and games from Apple, Atari, Commodore and others. By the mid-1970s, many vendors offered enhanced 8-bit architectures, with Zilog's Z80 being the most enduring. Two 1975 devices that presaged important later trends included a CMOS MPU from RCA (**PAGE 27**) and John Cocke's 801 RISC chip at IBM.

Beginning in the mid-1970s, 16-bit MPUs emerged from General Instrument (CP1600), National (PACE), TI (TMS9900), and Zilog (Z8000). Boosted by the PC boom of the 1980s, Intel's 8086/8088 (IBM PC) and Motorola's 68000 (Macintosh) devices enjoyed the greatest financial success.



Intel Corporation

↑ Gold interconnects highlight the i4004 layout complexity



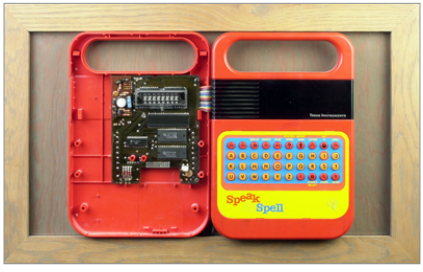
CHM collection: Gift of Federico Faggin

↑ Internal view of the MCS-4 chip set including the 4004 CPU in the Busicom calculator

1974

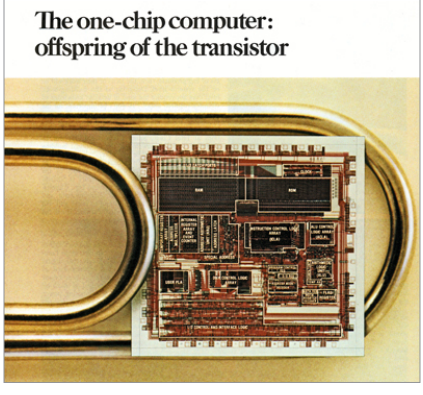
PAGE 44

General-purpose microcontroller family is announced



Texas Instruments, Inc.

↑ The TMS 1000 powered the Speak and Spell educational toy



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↑ Bell Labs' ad shows the MAC-4 die relative to a paperclip

A single-chip calculator design emerges as the TMS 1000 micro-control unit or MCU, a concept that spawned families of general-purpose digital workhorses that power the tools and toys of the developed world.

A microcontroller unit (MCU) comprises the same basic ROM, RAM and CPU elements as a microprocessor (MPU) for less demanding tasks such as controlling a toy or a microwave oven. As these applications do not require the ultimate in speed or program complexity, MCU designs can be implemented with fewer components so that the complete function will fit on a single chip.

Gary Boone and Michael Cochran's 1971 design of Texas Instruments TMS1802 single-chip calculator device provided the foundation for the TMS1000 general-purpose 4-bit MCU family announced in 1974. Priced at $2 in volume, it powered burglar alarms, garage door openers, games, and toys such as "Speak and Spell" that introduced digital electronics to the consumer.

In 1976, both Intel and Mostek (3870) introduced 8-bit architectures that served more demanding applications in automobiles and PC peripherals. The Intel MCS-48 family offered both EPROM (8748) and masked-ROM (8048) versions. The EPROM version made MCUs practical for prototyping and low-volume production systems. (PAGE 42) Intel's more powerful 1980 successor, the 8051, established a standard architecture that survives today in numerous variants for specific applications.

By the 1980s, MCU architectures from European, Japanese and U. S. manufacturers served numerous special-purpose applications. Bell Laboratories' MAC-4 met telecommunications needs. Motorola and Hitachi derived high-performance MCUs from the 68000 MPU. General Instrument's PIC family (today Microchip) won low-cost consumer designs. Hidden by the hundreds in appliances, automobiles, and personal electronics products, the MCU may be today's most ubiquitous semiconductor device.

Scaling of IC process design rules is quantified

1974

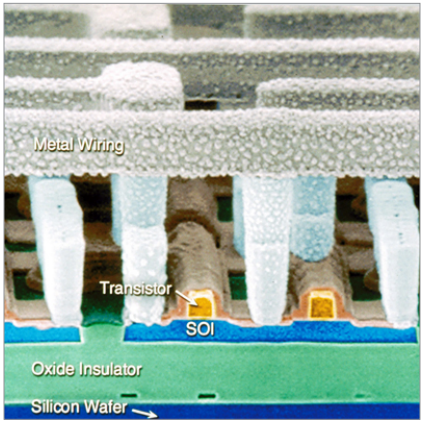
PAGE 45

IBM researcher Robert Dennard's paper on process scaling on MOS memories accelerates a global race to shrink physical dimensions and manufacture ever more complex integrated circuits.

Linear shrinking of mask dimensions with each advance in lithographic capability provided a quick fix to enhance the speed and reduce the cost of ICs in the 1960s. Thomas Stanley of RCA Research Laboratories published an analysis in 1962, noting that this was particularly relevant to the MOS transistor because its critical speed limiting dimension, the length of the gate, lay in the horizontal rather than the vertical plane of bipolar devices.

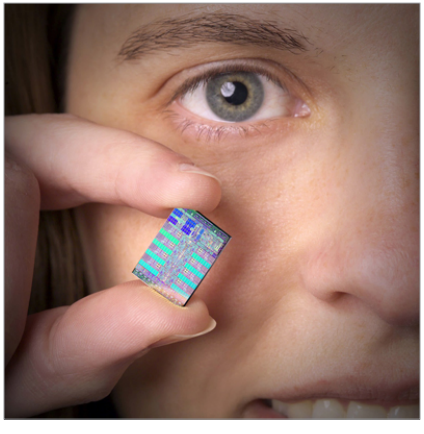
Scaling principles were described in 1972 papers by Bruce Hoeneisen and Carver Mead of Caltech and by IBM's Robert Dennard and his colleagues. But it was a 1974 paper by Dennard *et al.* that caught the attention of the industry with a resulting profound effect on microelectronics. They noted that as the horizontal dimensions of a transistor were scaled by a factor, speed improved by that same factor. At a time when IBM's MOS memories used a minimum dimension of 5 microns, they projected shrinking to fractions of a micron. (A human hair is 50–100 microns in diameter.) This was the first attempt to relate a geometry shrink to the resulting power reduction and performance gain. It gave Gordon Moore's "Law" (**PAGE 32**) a scientific foundation.

In 1976, MITI organized Hitachi, NEC, Fujitsu, Mitsubishi and Toshiba into a consortium, the VLSI Technology Research Association, that embraced the concept of scaling and combined it with Japanese optical and ultra-clean manufacturing strengths in a global race to deliver 64K DRAMs (**PAGE 41**) by the end of the decade. Power consumption at these high transistor counts accelerated the adoption of CMOS technology (**PAGE 27**). The ability to scale CMOS allowed dimensions to shrink below 100 nanometers (0.1 micron) by 2006 and to deliver chips such as the IBM/Sony/Toshiba 234 million transistor Cell processor for the Playstation 3.



Courtesy of International Business Machines Corporation

↑ SEM image of a sub-100 nm CMOS transistor



Courtesy of International Business Machines Corporation

↑ 234,000,000 transistor Cell processor for Playstation 3

Epilog

The year 1959 saw an extraordinary burst of intellectual activity across the semiconductor industry aimed at solutions to the challenge of integrating multiple devices on a single chip. Jack Kilby of Texas Instruments, along with Jean Hoerni and Robert Noyce of Fairchild Semiconductor, Kurt Lehovec of Sprague Electric, and others, filed patent applications that held keys to the development of the monolithic integrated circuit. Jay Last's team at Fairchild, which would create the first planar integrated circuits, also began their efforts in 1959.

Fifty years later, semiconductor manufacturers are delivering chips containing over one billion transistors. More transistors are produced every year—and at a lower cost—than grains of rice. The products and services enabled by this ubiquitous access to computing power have changed every aspect of the daily lives of citizens of the developed world. While the milestones selected from *The Silicon Engine* online exhibit and presented in this booklet terminate in 1974, they laid the foundations for succeeding developments that led to the integrated circuits of today.

Acknowledgements

Publication of this booklet is made possible by the generous support of the following sponsors and partners of the Computer History Museum's *Salute to the Semiconductor* program:

- Chemical Heritage Foundation
- IEEE, Santa Clara Valley Section
- Intel Corporation
- The House Family Foundation
- The Gordon and Betty Moore Foundation
- National Semiconductor Foundation, a charitable fund at the Silicon Valley Community Foundation
- Donors to the Silicon Industry Legacy Fund (SIL), including Applied Materials, Fairchild Semiconductor, KLA-Tencor, Lam Research, Linear Technology, National Semiconductor, and Xilinx.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Milestones in the development of transistors and integrated circuits selected from The Silicon Engine *online exhibit*